ECE 201/401: Advanced Computer Architecture

**Instructor:** Prof. Michael Huang, CSB 414, Office hour (3:00-4:30pm, Th)

**TAs:** Aaron Carpenter and David Toub

**Course Descriptions/Objectives:**
Introduction to principles and practices of modern high-end microprocessor design.

Topics covered:
1. Computer design concepts, principles, and quantitative methodologies of design evaluation
2. Instruction set design
3. Advanced processor pipelining
4. Software and hardware exploitation of instruction-level parallelism
5. Memory hierarchy design
6. Multiprocessor issues
7. Storage and interconnection

The lectures will be focused on qualitative concepts. Homework and lab assignments are essential for understanding the tools and quantitative methodologies of processor design.


**Homework and Lab Policies:** Submission of homework and lab assignments are controlled by WebCT. Policies are thus automatically enforced. Submission after the cut-off date is not accepted by the server. Frequent late submissions will result in penalties in the final grade calculation.

**Academic honesty:** Any form of dishonesty in an assignment results in a grade of 0 in that assignment plus a severe penalty. A second incident results in failure of the course.

**Grading:** HW/Lab/Quizzes 30%, mid-term 25%, final (comprehensive) 40%, presentation 5%, participation/interaction 5% (extra)
<table>
<thead>
<tr>
<th>No.</th>
<th>Date(s)</th>
<th>Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>9/5</td>
<td>Introduction to ECE 201/401</td>
</tr>
<tr>
<td>2</td>
<td>9/7</td>
<td>Lecture 1: Fundamentals of Computer Design and</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Lecture 2: Instruction Set Architecture</td>
</tr>
<tr>
<td>3,4</td>
<td>9/12, 14</td>
<td>Lecture 3: Review of Pipelining</td>
</tr>
<tr>
<td>4-7</td>
<td>9/14, 19, 21, 26</td>
<td>Lecture 4: ILP and Its Dynamic Exploitation</td>
</tr>
<tr>
<td>8-11</td>
<td>9/28, 10/3, 5, 10</td>
<td>Lecture 5: Exploiting ILP with Software Approaches</td>
</tr>
<tr>
<td>12</td>
<td>10/12</td>
<td>Lecture 6: Memory Hierarchy Design</td>
</tr>
<tr>
<td>13</td>
<td>10/17</td>
<td>(buffer)</td>
</tr>
<tr>
<td>14</td>
<td>10/19 (in-class)</td>
<td>Midterm: Includes Lectures 1-4 and the</td>
</tr>
<tr>
<td></td>
<td></td>
<td>first half of Lecture 5 (Ch 4.1, 4.2)</td>
</tr>
<tr>
<td>15-18</td>
<td>10/24, 26, 31, 11/2</td>
<td>Lecture 6: Memory Hierarchy Design (cont)</td>
</tr>
<tr>
<td>18,19</td>
<td>11/2, 7</td>
<td>Lecture 7: Storage Systems</td>
</tr>
<tr>
<td>20-25</td>
<td>11/9, 14, 16, 21, 28, 30</td>
<td>Lecture 8: Multiprocessor and Thread-Level Parallelism</td>
</tr>
<tr>
<td>26</td>
<td>12/5</td>
<td>Lecture 9: Interconnection Networks &amp; Clusters</td>
</tr>
<tr>
<td>27</td>
<td>12/7</td>
<td>Lecture 10: Final Review</td>
</tr>
<tr>
<td>28</td>
<td>12/12</td>
<td>(buffer)</td>
</tr>
<tr>
<td></td>
<td>12/20 (12:30-3pm)</td>
<td>Final Exam (Comprehensive)</td>
</tr>
</tbody>
</table>

Note: The schedule is subject to change depending on the progress. Certain sessions may be canceled or rescheduled due to conference travel etc.