Abstract—The operation principle of single-electron devices (SEDs) is reviewed. Single-electron box, transistor, and trap are presented. Current SED applications are introduced, particularly silicon single-electron memory and logic. SED implementation challenges and future research are proposed.

Index Terms—single-electron device; single-electron box; single-electron transistor; silicon single-electron memory; silicon single-electron logic.

I. INTRODUCTION

SINGLE electron devices (SEDs) are based on the controllable single electron transfer between small conducting “islands”. In 1909, Millikan first illustrated the manipulation of single electrons; however the single-electron device cannot be implemented in solid state circuit until late 1980s, due to limited fabrication techniques. SEDs have already been applied in several important scientific experiments [6-8] and are feasible in unique scientific instrumentation and metrology. In addition, some exciting ideas may revolute logic and memory design in silicon-based circuit design area [9, 10]. Furthermore, it has been shown the promising future that replacing silicon transistors with single-electron transistors (SETs) [6, 8, 11-14].

II. OPERATION PRINCIPLE

A. Basic Physics

Assume a small metal sphere (also called island, shown in Fig.1) which is been electroneutral initially, i.e. zero net charge. In this state, no electrical field occurs beyond the border of the island. When an external force \( F \) brings a single electron \((-e)\) from outside close to the island, an electrical field \( \epsilon \) is generated by the nonzero net charge. The electrical field is oppositely proportional to the square of the island size, so it may become very strong for nanoscale structures [1], [2].

Charging energy \( E_c \) is a more accurate measurement on this charge effect than electrical field. As the island size is comparable with the de Broglie wavelength of the electron island, the energy scale is described by electron addition energy \( E_a \), the sum of charging energy \( E_c \) and quantum kinetic energy of the added electron \( E_k \). To reduce the thermal fluctuation impacts on \( E_k, E_c \) should be the dominant of \( E_a \). Generally speaking, the digital single-electron devices operating at room temperature require \( E_a \) few electron-volts and minimum feature size \(~1\) nm, so that thermally-induced random tunneling events can be avoided.

B. Orthodox theory

Reference [3] formulated the orthodox theory of single-electron tunneling, which plays an important guiding role in the history of single-electronics. A single electron randomly tunnels through a particular tunnel barrier with a certain rate \( \Gamma \), which depends on the electrostatic energy reduction of the system as a result of this tunneling event, as shown in Fig. 2. This is because the rate is proportional to the number of occupied quantum states in the electron source.

III. TYPICAL SINGLE-ELECTRON DEVICES

A. Box

Single-electron box is the conceptually simplest device. As shown in Fig. 3 (a), it is composed of a small island, which is
separated from a large source electrode by tunnel barrier. Gate electrode is another electrode, which is used to apply an external electrical field on the small island. As the electrochemical potential of the island is changed by the external electrical filed $E$, electron tunneling effects occur through the tunnel barrier. The free energy (Gibbs) energy of the system is illustrated in (1). The island charge $Q$ is a step function of the applied voltage $U$, as defined in (2) and (3). Here, $C_0$ and $C_g$ are the island-gate capacitance and total capacitance, respectively. $Q_e$ is the external charge. The increasing gate voltage $U$ leads to more electrons on the island.

$$W = Q^2 / 2C_e + (C_0/C_g)QU + \text{const}$$

(1)

$$Q = ne - Q_e$$

(2)

$$Q_e = UC_0$$

(3)

However, two major drawbacks prevent single-electron box from being an electronic circuit component [6]. (1) This structure cannot store information, because the charges stored in the island are a function of applied voltage $U$; (2) it is hard to measure its charge state, due to no dc current carried in the box.

### B. Transistor

1) **Coulomb blockade**

The schematic of the single electron transistor with biased voltages is shown in Fig. 4. First assume the gate voltage $V_g$ is zero. If the biased voltage $V_b$ is less than the threshold voltage $V_C = \epsilon/C_g$, no electron can tunnel through the two tunnel junctions, because there is not sufficient energy to charge the island. This behavior is so called **Coulomb blockade**. When $V_b$ is greater than $V_C$, current will flow through the circuit as shown in Fig. 5 (a). The charge $q$ contained in the whole island is as follows:

$$q = -q_1 + q_2 + q_0 = -ne + q_0$$

(4)

Here, $q_0$ is the background charge, which is non-integer and resulted from impurity, and $\epsilon$ is the electron charge.

![Coulomb blockade schematic](image)

### C. Trap

Single-electron trap has more than two tunnel junctions in the island, which is separated by tunnel barriers [7, 8]. This device operates like an internal memory, and can store two or more bits of information by changing $V_g$ applied on the device’s island, as shown in Fig. 6. First, the gate electrode is provided with a sufficiently high gate $U^+$, and the electrons are driven into the edge island. Then, $V_g$ is decreased to the initial level, so the electrons are trapped in the island. By reducing voltage further, the electrons can be removed from the trap. However, the lifetime of a certain state is basically constrained by the thermal activation over the energy barrier and co-tunneling.
IV. SINGLE-ELECTRON DEVICE APPLICATIONS

A. Memory

Currently, SED memories have become the most important SED application, for either electron storage or charge sensing. Because of small dimensions, the SED is very promising for high density memory design. In addition, memory usually has a periodic and simple structure, so it is possible to implement memory with SEDs.

However, the background charge is too random to be employed in VLSI circuits, which is proved by the statistical distribution of the Coulomb blockade threshold and the energy barrier height of the island array. In addition, the background charge also leads to the unreliability of the SET readout. The charge trapped in the island can be easily imitated by a random charged impurity [9].

Single-electron transistor/field electrical transistor hybrid design (SET/FET hybrid) is a background-charge-insensitive memory. The minimum feature of this memory is about 3 nm, which is much larger than the requirement for single-electron digital circuits. And the absence of storage capacitor inside the memory makes it more attractive for high density purpose. The main drawbacks are slow write process and insensitive to the applied voltage. Crested tunnel barriers are proposed to overcome those disadvantages, at the cost of fabrication difficulty.

Experiments turn the theoretical models into reality. K. Yano et al. [10] showed single electrons are captured in the channel of certain stand-alone grains. Its main disadvantage is inherently irreproducible. S. Tiwari at IBM [11] separated the electron-capturing island and a MOSFET channel, which overcome the granular limitation on the channel.

B. Logic

The SET is the primary device to substitute the MOSFET in conventional logic gates. Although Coulomb blockade and single-electron tunneling are dominant phenomena in single-electron circuits, they cannot generate currents directly. Basically, single-electron device logics have two categories: SET-based logic and charge state logic [9]. The current of the former one is produced by the sequence of single-electron tunneling. The corresponding bit is represented by the voltage, which is generated by the accumulation of plural electrons. Si-based researches on SET-based logic circuits, such as Invertor, NAND and XOR gates, have been demonstrated. In contrast, the bit of the charge state logic is represented by the elementary charge. The representative devices are quantum cellular automation (QCA) and single-electron binary decision diagram (BDD) [11-14].

V. CHALLENGE AND CONCLUSION

SEDs have shown promising applications in metrology, terahertz radiation diction and imaging. Because of natural small dimension, SED is a potential solution for continue silicon scaling. In addition, low power dissipation can be achieved in circuits composed of single-electron devices.

Metallic structures can be fabricated with vertical and lateral islands and tunnel barrier structures at temperature up to 77K. GaAs and silicon based SEDS have been already demonstrated. However, fabrication is still the most difficult challenge of SED application. Electron beam lithography and scanning probe techniques offer the best prospects for the future. Besides, some more esoteric techniques based on atomic particle deposition and colloid chemistry may also provide some benefits.

REFERENCES