Abstract: I will describe novel thin film electronics, based on metal-oxide materials, with architectures that are enabled by spatial Atomic Layer Deposition (SALD). SALD is a deposition process performed at atmospheric pressure that can grow coatings very quickly. In one approach we fabricate devices using selective area deposition, with inkjet-printed inhibitor, to additively pattern all the active layers. We build full transistors and circuits using one inhibitor ink, the SALD system, and an oxygen plasma to clean the substrate. Performance of the resulting transistors and circuits match photolithographically patterned ones, with mobility above 10 cm²/V-s, but the digital design allows us take a desktop layout to completed circuits in hours. In the second approach we use the well-known conformality of ALD to build self-aligned, sub-micron channel length, vertical transistors. The vertical transistor electrical performance is impressive compared to amorphous silicon TFTs, for example, yet the alignment tolerances inherent in the fabrication process are large. We discuss materials and device design considerations for each of these approaches. Acknowledgment: Carolyn Ellinger, and Lee Tutt

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