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**Characterization and Modeling of TSV Based
3-D Integrated Circuits**

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Through-silicon via (TSV) based three dimensional integrated circuits have rapidly progressed over the past decade. TSV based three-dimensional integration not only has the potential to boost the performance and capabilities of state-of-art integrated circuits, but supports the integration of completely disparate technologies. Three-dimensional integration provides a different perspective to traditional system-on-chip (SoC) circuits, where each device plane can be a different and fully optimized technology rather than multiple technologies merged onto a single 2-D plane.

Three-dimensional integration has progressed significantly over the past decade, and although manufacturing hurdles remain, greater emphasis has recently been placed on design considerations for 3-D ICs. The constraints on 3-D integrated systems stem from the lack of design expertise and proper design tools for integrating multiple device planes, some of completely different technologies. Although manufacturing techniques have been developed to alleviate thermal hot spots caused by stacking device planes, design tools are just beginning to incorporate models and analysis methodologies addressing this concern. In addition, multi-plane synchronization and power delivery, although topics of serious research over the past decade, require further advancements, with the need for novel design techniques and methodologies that consider multiple voltages, frequencies, and power demands of the various device planes.

The work presented here provides insight into some of the more pressing design issues being addressed by the research community at large, and provides guidelines for designing these evolving TSV based 3-D technologies. In particular, there is a focus on clock and power delivery in 3-D systems, as well as an analysis of the electrical properties of the TSV. In addition, thermal properties, including generation and spreading of heat within 3-D integrated circuits, are explored.

The organization of the dissertation begins with an introduction to TSV electrical models, power delivery, and thermal impacts and mitigation techniques for 3-D ICs. After background material required for the rest of the dissertation is provided, characterization and physical design methodologies for 3-D integrated circuits are discussed. Electrical modeling of TSVs is presented, culminating in the development of closed-form expressions of the TSV resistance, capacitance, and inductance. Errors of less than 2% between the closed-form models and simulations are demonstrated for both the resistance and inductance of a 3-D via. Errors of less than 8% for the capacitance are also reported.

Models of three distinct clock distribution networks are provided, and a comparison of the power and delay of each topology is described. The per cent error between the model and experimental clock delays is determined for the three clock topologies. A maximum error of less than 10% is achieved for the clock paths within the H-tree topology.

A noise analysis of three power delivery topologies is presented, with experimental evidence indicating the effect of the through silicon via (TSV) density on the noise profile of a 3-D power delivery network. A comparison of the peak noise for each topology with and without board level decoupling capacitors, and resonant behavior are provided, and suggestions for enhancing the design of a 3-D power delivery network are offered. Based on the experimental results, noise is reduced by 2% to 14.2% by doubling the number of TSVs and utilizing a dedicated power and ground plane. The area penalty for increasing the number of TSVs on the power network from 576 to 864 is an additional 0.68% of the 530 μm by 500 μm area occupied by each power distribution topology on each device plane. Models of the three topologies indicate resonant behavior at around 200 to 225, 450, 700 to 800, and 1250 to 1800 MHz, depending on the impedance characteristics of the cables, board, wirebonds, and particularly the on-chip power distribution networks.

Thermal properties including generation and spreading of heat in 3-D integrated circuits are discussed as part of a larger project exploring a promising application of 3-D ICs: the development of a 3-D integrated free-space optical interconnect system for multi-core communication, a merging of semiconductor device planes with optical devices. The operation of vertical-cavity surface emitting lasers (VCSELs) for the free-space optical interconnect system increases the temperature of the 3-D IC. Thermal models of bundled VCSELs indicate the maximum internal temperature of the VCSEL arrays can range from 306.5 K for a 20 μm D_a , 100 μm substrate thickness, 666 A/cm² current density, and 1 \times 1 array size to 412 K for a 5 μm D_a , 300 μm substrate thickness, 1200 A/cm² current density, and 4 \times 4 array size. In addition, the location of a die in a 3-D IC significantly affects the peak temperature of the device plane. The maximum observed temperature on a die increases by 65.7% when the heat source is active on a bottom device plane as compared to a heat source on a device plane with a surface interfacing air (from 60.9° C to 100.9° C). The placement of two highly active circuit blocks aligned directly above one another also has a significant effect on the thermal profile of an entire 3-D IC. A 79.4% increase in temperature is observed (from 69.6° C to 124.8° C) when two active circuit blocks are aligned in the vertical direction.

Three-dimensional integration is an evolving technology that will prolong the semiconductor roadmap for several generations. Opportunities abound with improvements in performance and functionality of traditional silicon based circuits, as well as the potential to merge exotic technologies into a single integrated circuit. During the past decade, considerable progress has been made in manufacturing 3-D circuits; design methodologies however, have lagged these technological advancements. The objective of this dissertation is to provide insight and design expertise, with a goal of strengthening the design capabilities for 3-D integrated circuits.