Abstract—In this paper, leakage mechanisms in ballistic deflection transistors (BDT) are studied using Finite Element Analysis (FEA) based on a simple conductive media model, a BDT simulator based on the semi-classical billiard model, and experimental measurements. In BDT, by simply tailoring the architecture, the electron transport can be, to a large extent, modified and controlled to reduce leakage. Since the triangular deflector plays a significant role in the operation of BDT, the models take into account its position variation along the Y-axis. Experimental results also discuss leakages with the deflector position (DP) variation. Structural modifications in the BDT help in analysing the device functionality, and understanding the relationship between right drain output current ($I_{RD}$), left drain output current ($I_{LD}$) and top drain leakage currents ($I_{TD}$) with device geometry.

Index Terms – Ballistic Transport, Leakage Current, Deflector, Comsol Modeling, Billiard Model, Experiments.

I. INTRODUCTION

To achieve high performance and higher functional integration density of digital devices, CMOS devices have been scaled down aggressively in each technology generation. However, the leakage current has increased drastically with technology scaling, because of tunneling through the gate dielectric as well as the junctions of the transistors, essentially limiting further development. The power dissipation of CMOS circuits has increased, as threshold voltage, channel length, and gate oxide thickness have been reduced.

With the advancement in nanofabrication processes, device dimensions smaller than mean-free path can be realized. At this scale, operational behavior of these devices changes qualitatively from diffusive (Ohmic) to ballistic (non-Ohmic) transport. A number of device concepts and geometries have been generated based on ballistic electron transport, but only a few have been demonstrated to work at room temperature. Büttiker-Landauer theory describes the ballistic nature of these devices at low temperature [1], [2], but starts losing its significance as the temperature rises.

The increasing statistical variation in parameters such as material system configuration, supply voltage, geometry and temperature, has emerged as a serious problem in nano-scaled circuit design and can cause significant increase in the device leakage current. The performance of ballistic devices can be improved by optimizing the geometry, in addition to the lithographic techniques and material system configuration. It is hence possible to generate new device functionalities and properties by simply tailoring the device shape. In particular, it was recently realized that the geometrical symmetry of a ballistic device can also have a profound influence on the nonlinear device properties [3]. In contrast, due to the nature of the diffusive electron transport, the properties of a traditional device are not as much sensitive to a change in the device boundary.

Ballistic devices, due to their planar structure, are much more prone to various kinds of leakages. The layered structure may help charges to diffuse from one layer to another, which causes an uneven distribution of these charges at the terminals, and changes the current density at the electrodes. With modeling tools, it is convenient to discuss leakage and output current issues of the device, and furthermore these theoretical results can be realized by the actual experimental measurements. In this paper, we discuss leakage mechanisms in the BDT as a function of its architecture (specifically deflector position) since its performance significantly depends on its geometry [8]. Modeling and experimental results are studied to examine the device response to deflector position variation. It is observed that the output and leakage current depend significantly on deflector position. It is noticed that the leakages and output are of same order of magnitude and thus are comparable for various positions of deflector.
II. BDT OVERVIEW

Our group first proposed BDT in [4], which presents a Terahertz transistor. A SEM image of the BDT is shown in Fig.1. The BDT is based upon electron steering, and the ballistic deflection effect. Differential input voltages, applied to the in-plane gates, provide a lateral electric field which directs electrons to either the left or right drain. These outputs (IRD and ILD) depend on the gate bias, and are either complementary or non-complementary. This facilitates a wide variety of circuit design techniques. The deflector aids in directing current into one of the output channels, and reduces ITD. Since the typical mean free path of the 2DEG at 300 K in a compound III-IV semiconductor is 100-200 nm, the material system chosen is lattice matched layers of InGaAs and InAlAs on an InP substrate. This provides a larger mean free path and higher mobility, allowing ballistic behavior at room temperature [5]. In Fig.1, the bright area represents the 2DEG, and the dark regions including the triangle are removed material from the 2DEG structure. The 2DEG has high electrical conductivity, whereas dark areas are non conductive. The passivation layer material between the channel and the gates is air. A theoretical frequency (\(f\)) of 1.02 THz is estimated with the microstrip approximation, where the capacitance calculated between channel and gate is 7.02 aF [5].

The BDT produces far less heat and runs much faster than standard transistors, because it does not start and stop the flow of electrons the way conventional designs do [4]. A simple operational mechanism of the BDT exhibits that when the electron current moves along the right drain, the transistor registers logic “1”, and when the electron current moves along the left drain, it registers logic “0”. A traditional transistor registers a “1” as a collection of electrons on a capacitor, and a “0” when those electrons are removed. Moving electrons on (charging) and off (discharging) the capacitor takes time. This refill time limits the speed of the transistor. A second drawback is that conventional transistors produce immense amounts of heat when that energy is emptied. But as there is no such mechanism associated with BDT, it is expected to run much faster than the conventional transistors, with little heat produced during operation.

The deflector is one of the most significant structures in the BDT. The performance of BDT depends on the sizing and position of the deflector. As we reduce the scale, a larger percentage of electrons will interact with the artificial scattering object ballistically. This should produce an effect similar to the ballistic bridge rectifier [6]. Differential input voltages on the gates are applied, which ultimately results in non-linearity of the device. The non-linear change in potential is due to electrons being deflected away from the center drain port by the artificial scattering mechanism, the gate control over the channel can be attributed to two effects, classic channel pinch-off due to field effect, and an electron steering effect. The steering effect implies the flowing electrons encounter a lateral field directing them towards one channel or the other, depending on gate bias. Pinch-off can be observed when a strong bias depletes the channel completely. Since there are both pinch off and steering effects, the transconductance of the device can be either positive or negative depending upon the gate voltage.

III. THEORETICAL STUDY OF LEAKAGE MECHANISM

Various simulation techniques and modeling tools have been used for the study of BDT [7]. It has been observed that the performance of BDT significantly depends on its geometry [8]. The BDT device was simulated using Finite Element Analysis (FEA), based on a simple conductive media model, solving the equation,

\[
\nabla \left( \sigma \nabla V - J \right) = Q
\]

where \(\sigma\) is electrical conductivity, \(V\) the electric potential, \(J\) an externally applied current, and \(Q\) is any internally generated current. For purposes of our model, \(J\) and \(Q\) are both zero. The conductivity of the 2DEG was approximated based on a carrier density of \(10^{12} \text{ cm}^{-2}\), and the InGaAs bulk electron mobility of 12,000 \(\text{cm}^2/(\text{V} \cdot \text{s})\), giving a value of 0.00192 S for \(\sigma\). Comsol Multiphysics\textsuperscript{TM}, an FEA software package, was used to perform the simulation. Although this approach does not attempt to rigorously model the physics of the device, it is still useful if the results are well correlated to experimental data.

The effect of applied gate voltage was modeled as depletion of the channel on the side of the negative electrode. The depletion was assumed to advance laterally across the channel, as a linear function of gate voltage, until complete pinch-off at the max gate voltage. Future work is to model the charge distribution and conductivity in the channel, as a function of gate voltage, both numerically using FEA, as well as analytically. The function of the
deflector in this FEA model was particularly of interest. Although it does not act as a deflector in the ballistic electron sense, it serves a similar function, in the sense that it redirects the flow of current. Its shape and position influence the distribution of output current between the top, left, and right electrodes. Ideally, all the current flowing into the device should contribute to the gain, and no current should flow out the top drain; however, in reality, leakage current ($I_{TD}$) occurs at the top port. Fig. 2 shows the placement of deflector and its distance from source port which is denoted by “k”. The different values chosen for k are 210nm; 245nm; 280nm; 315nm and 325nm. At k = 315 nm, the deflector is at a distance of 10 nm from the top port, which is close to the Vdd opening yet it does not block the flow of electron towards top drain. Thermionic injection may increase the leakage for this case; however, the conductive media model is simple, and does not account for this effect. The results of the model indicate that even without tunneling, the conductance of the 2DEG may be sufficient to account for the measured leakage.

Table 1 shows that $I_{LD}$ and $I_{RD}$ are almost equal for each k. Also for all deflector positions, $I_{TD}$ is comparable to the output currents except for k=325 nm where the deflector is actually closing the top port completely.

**TABLE 1**

<table>
<thead>
<tr>
<th>k(nm)</th>
<th>$I_{LD}$(Ampere)</th>
<th>$I_{RD}$(Ampere)</th>
<th>$I_{TD}$(Ampere)</th>
</tr>
</thead>
<tbody>
<tr>
<td>210</td>
<td>1.57926E-04</td>
<td>1.57921E-04</td>
<td>1.21085E-04</td>
</tr>
<tr>
<td>245</td>
<td>1.81166E-04</td>
<td>1.81166E-04</td>
<td>1.30917E-04</td>
</tr>
<tr>
<td>280</td>
<td>1.93223E-04</td>
<td>1.93229E-04</td>
<td>1.28672E-04</td>
</tr>
<tr>
<td>315</td>
<td>2.10844E-04</td>
<td>2.10841E-04</td>
<td>9.08827E-05</td>
</tr>
<tr>
<td>325</td>
<td>2.3657E-04</td>
<td>2.44E-04</td>
<td>2.97E-12</td>
</tr>
</tbody>
</table>

Fig. 3 compares $I_{TD}$ leakage and $I_{LD}$ output with k. $I_{TD}$ and $I_{LD}$ are not shown at k=325 nm, since at this position, leakage becomes negligible through the top port. For all other k values, it is observed that the left output increases with k. The behavior of the right output with k is similar to $I_{LD}$. It is also noticed that as the deflector shifts towards the top drain, leakage first increases and then decreases, following a quadratic behavior along the Y axis, due to uneven electron distribution. This behavior can be attributed to the fact that when the deflector is far from the top drain opening, closer to the bottom channel, it most effectively steers current to the left or right. As the deflector moves towards the top channel, the steering effect begins to decrease, so leakage current increases. When the deflector gets close to the top drain opening, leakage again reduces significantly as resistance is increased by the narrowing of the opening.

Fig. 4. Theoretical effect of k changes on leakage current.

Optimization in the size and position of the deflector is imperative for optimum performance of the BDT. Figure 4 shows that our modeling results are consistent with [9]. It shows that leakage will decrease for deflector positions that are closer to the top or bottom, and increase as the deflector moves to the middle. Fig. 4 shows that when the push-pull differential gate voltage is applied, leakage becomes minimum for k=325 nm, which is expected since the deflector has closed the path. The next lowest leakage occurs.
at \( k = 315 \) nm which is, again expected because the distance between deflector and top port is just 10 nm, which increases the resistance.

It is important to look at the difference between output and leakage to know the power dissipation of the device for different \( k \) values. Fig. 5 shows the current-leakage difference variation with \( k \). It is observed that with \( k \), the difference increases. This behavior is attributed to the fact that as the deflector shifts towards top port, the top port is almost closed, and fewer electrons are now passing through it. When the deflector closes the top port completely, the difference becomes maximum. In that case the left output is \( 2.3657E-04 \) and the difference is \( 2.3656999E-04 \) which indicates that the difference is nothing but ~ left output.

**IV. SIMULATION RESULTS FROM BDT SIMULATOR**

To facilitate the investigation of the BDT properties, we proposed a multi-purpose simulator for ballistic nanostructures, based on a simplified semi-classical ballistic transport model [9]. Using this Monte Carlo simulator (shown in Fig. 6), we examine the impact of the deflector position changes on the leakage current. As shown in table 2, \( I_{LD} \) is close to \( I_{RD} \), which is consistent with the results obtained from the FEA model. Similarly, \( I_{TD} \) is comparable to the left output and right output currents for the deflector position far away from the top port. As the deflector moves up towards the top terminal, the leakage current significantly decreases, although the leakage current reduction caused by increasing deflector position is not as significant as that obtained from the FEA model. This is because we initialize a certain number of electrons in the device at the beginning of simulation, and those electrons contribute to the non-zero leakage current.

Fig. 7 depicts \( I_{LD} \) and \( I_{TD} \) with different deflector positions. The increasing deflector position first results in the increase of \( I_{LD} \), which is similar to the phenomena observed in the FEA model. When the deflector further moves up, the current moderately decreases, as shown in Fig. 7(a). If the differential gate voltage increases to 1 Volt, the random effect on the simulation result is significantly reduced, as shown in Fig. 7(b).

**TABLE 2**

<table>
<thead>
<tr>
<th>( k(\text{nm}) )</th>
<th>( I_{LD}(\text{Amperes}) )</th>
<th>( I_{RD}(\text{Amperes}) )</th>
<th>( I_{TD}(\text{Amperes}) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>185</td>
<td>5.384E-6</td>
<td>5.592E-6</td>
<td>1.182E-5</td>
</tr>
<tr>
<td>205</td>
<td>2.209E-5</td>
<td>2.171E-5</td>
<td>1.915E-5</td>
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<td>235</td>
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<tr>
<td>250</td>
<td>3.724E-5</td>
<td>3.516E-5</td>
<td>1.137E-5</td>
</tr>
<tr>
<td>265</td>
<td>3.379E-5</td>
<td>3.461E-5</td>
<td>1.066E-5</td>
</tr>
<tr>
<td>300</td>
<td>2.249E-5</td>
<td>2.506E-5</td>
<td>1.033E-5</td>
</tr>
<tr>
<td>320</td>
<td>1.772E-5</td>
<td>1.733E-5</td>
<td>9.376E-6</td>
</tr>
<tr>
<td>335</td>
<td>1.699E-5</td>
<td>1.754E-5</td>
<td>5.120E-6</td>
</tr>
</tbody>
</table>

**Fig. 6 Interface of our Monte Carlo simulator**

**Fig. 7 Modeling comparison of \( I_{TD} \) and \( I_{LD} \) with \( k \).**

(a) Differential gate voltage = 0 Volt

(b) Differential gate voltage = 1 Volt
Consequently, trends of both $I_{LD}$ and $I_{TD}$ versus deflector position are close to those shown in Fig. 3. Note that our simulation result also shows that increasing deflector position cannot endlessly boost the left drain current; instead, there is a saturation point for maximum left output. In our previous work [9], we illustrate the impact of the differential gate voltage on the top drain leakage current, which is consistent with Fig. 4.

The difference between the output current and leakage is shown in Fig. 8. The current difference increases with the increasing deflector position, except two positions that are very close to the top port. This inconsistency is caused by two reasons—(1) the saturation of the left drain current, (2) the electrons initialized in the 2DEG at the beginning of our Monte Carlo simulation. In future work, we will eliminate this limitation to simulate more realistic behaviors.

V. EXPERIMENTAL RESULTS EXPLAINING LEAKAGE

It is imperative to compare models with experimental results in order to know the authenticity of the obtained results. The BDT has been modeled and experimentally tested before as well in [7] and [8]. In this section we are comparing the results obtained through Comsol modeling, semi-classical billiard modeling and experimental measurements. BDTs of different dimensions and shape were fabricated on separate runs and experiments were performed with different deflector position values. The fabricated devices are larger in dimensions than the modeling dimensions. Considering the fact that the devices were larger in size, experimental results are qualitatively consistent with modeling results. Different dimensions used for the fabrication purpose are given in [8], except the change in deflector placement. Due to the larger BDT dimensions, the quantum effects have been washed away and now the device’s behavior is not ballistic but diffusive. But at the vicinity of deflector, where deflector-electron interactions take place, quantum effects occur which in a broader sense increases the speed of the device and thus produces the complementary output. Thus even bigger devices show ballistic behavior but only around deflector.

Table 3 shows the device performance due to the uneven distribution of charge at different electrodes. Here also, the deflector position is changed, but the $k$ values are different from that of the modeling $k$ values, since the device size is larger. The different $k$ values assigned for the experimental purpose is shown in table 3. It can be seen from the table that right and left drain output current is almost equal, and these outputs are comparable but larger than the top drain leakage current, which is expected. For $k=420$ nm, leakage becomes maximum, and the second lowest leakage occurs at $k=330$ nm, which confirms the fact that placing deflector above and below a specific position decreases the leakage [9].

Fig. 9 gives an experimental comparison and trend between output and leakage. Ideally, leakage can be minimized by closing the top opening (as in modeling), but in reality, fabrication limitations do not allow touching the deflector to the top port and keeping all the dimensions and shape of the device features stable at the same time (note that deflector is nothing but a hole down in the layers). Thus we cannot actually minimize the leakage this way. However, for a specific $k$ value the leakage can be reduced to its minimum, which is little larger than the theoretical minimum leakage. Fig. 9 shows that the output and top drain leakage follow the linear and quadratic behavior with $k$, respectively. On comparing Fig. 3 and Fig. 9, we found that the output variation with $k$ is less in experimental results. We designed and fabricated BDTs with deflector at different positions and noticed from Fig. 10 that leakage is maximum for $k=420$nm, which is $24\%$ of its length lower than the centre of the device which is again consistent with [9]. Placing deflector above or below $k=420$nm, decreases the leakage again.

<table>
<thead>
<tr>
<th>$k$ (nm)</th>
<th>$I_{LD}$ (Amperes)</th>
<th>$I_{RD}$ (Amperes)</th>
<th>$I_{TD}$ (Amperes)</th>
</tr>
</thead>
<tbody>
<tr>
<td>330</td>
<td>5.13E-06</td>
<td>5.12E-06</td>
<td>9.36E-07</td>
</tr>
<tr>
<td>420</td>
<td>5.78E-06</td>
<td>5.75E-06</td>
<td>7.39E-07</td>
</tr>
<tr>
<td>460</td>
<td>5.52E-06</td>
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<td>1.72E-06</td>
</tr>
<tr>
<td>500</td>
<td>5.93E-06</td>
<td>5.89E-06</td>
<td>1.25E-06</td>
</tr>
</tbody>
</table>

Table 3

**Fig. 9** Experimental comparison of $I_{TD}$ and $I_{LD}$ with DP.
At $k=500$ nm, a minimal leakage was expected since the distance between deflector and top port is too small, but we observed that the leakage was significant. This is due to the fact that at room temperature, the electron energy is greater than Fermi energy, thus thermonic injection of the electrons takes place allowing electrons to jump over the potential barrier to cause leakage. A general expression for the current density of electrons accounting for tunneling and reflection is given by (2)\cite{10} as

$$
J_{SD} = \frac{4\pi q k_B T}{h^3} \int_{E_C}^{\infty} T_i(E_x) m^*_T(E_x) \ln \left( \frac{1 + \exp \left( \frac{E_x - E_F}{k_B T} \right)}{\exp \left( \frac{E_x - E_F}{k_B T} \right)} \right) dE_x
$$

In equation (2), $J_{SD}$ is the current density of electrons injected from the source toward the drain, $q$ is electronic charge, $m^*_T$ is transverse effective mass, $k_B$ is Boltzmann constant, $T$ is temperature, $h$ is Planck’s constant, $E_F$ is the Fermi energy and $E_x$ is the electron energy. For the electron energy greater than the Fermi energy and potential barrier, the current density at room temperature given by (3) as

$$
J_{SD\text{therm}} \approx \frac{4\pi q m^*_T k_B^2 T^2}{h^3} \exp \left( \frac{E_C - \psi_B}{k_B T} \right)
$$

In equation (3), $J_{SD\text{therm}}$ is current density of electrons injected ballistically from source to drain over the potential barrier, $E_C$ is conduction band energy and $\psi_B$ is potential barrier. Fig. 11 shows that the difference between $I_{LD}$ and $I_{TD}$ is maximum when $k=420$ nm.

VI. CONCLUSION

Leakage mechanisms are studied using Finite Element Analysis, based on conductive media model, our Monte Carlo simulator based on semi-classical billiard model and experimental results. It is observed theoretically that leakage can be minimized by touching the deflector to the top port and thus closing the opening of the top port. It is also observed from FEA model that even for 10 nm distance between deflector and top port, the leakage is significant. The Billaird model concludes that the output saturates with increasing deflector position. Experimentally, it is observed that fabrication limitations do not allow the closing of top port with deflector, which actually forces designers to place deflector at its lowest position, closest to the source, to minimize the leakage at room temperature. It is also observed that placing the deflector lower and above a specific optimized position (420 nm in our case with given device specifications), decreases leakage.

REFERENCES