The DML static mode demonstrated the lowest energy dissipation: 2.2× less than CMOS on average, and 5× less than the domino. We presented a basic proof-of-concept of the proposed DML logic by measurements of an 80-nm test chip.

Future work will include the optimization of the DML gates for operation with standard supply voltages, development of a standard library and designing of a benchmark design using a standard ASIC flow.

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REFERENCES
Separate power networks can be designed to independently supply current to different parts of a circuit, thereby shielding different parts of an IC from each other. Separate power networks are widely used in mixed-signal circuits, where the current is supplied to the analog and digital circuits by different power networks [11]. For systems requiring the same voltage, this approach may, however, inefficiently utilize metal resources due to additional area and routing constraints [9]. Input/output (I/O) pads are also a limited resource, preventing the use of an excessive number of separate power networks [12].

In Fig. 1, a single and multiple separate power networks are illustrated. With a single network, as shown in Fig. 1(a), the sensitive circuit (e.g., a PLL) and aggressor circuit (exemplified by a large digital logic circuit) share the same power network that lowers the network impedance. A sensitive circuit can, however, be highly affected by the noise generated from the aggressor circuit. With multiple power networks, as shown in Fig. 1(b), one network can be dedicated to the aggressor circuit while another network can be dedicated to the sensitive circuits, minimizing noise coupling between the aggressor and sensitive circuits. This approach, however, results in an increase in the power network impedance and additional routability constraints. The methodology proposed in this brief utilizes a single power network to provide a low network impedance and reduced routability constraints while disconnecting (or breaking) links within the on-chip power network between the aggressor and sensitive circuits, thereby reducing the noise coupling to the sensitive circuits.

This brief is organized as follows. The link breaking methodology is described in Section II. In this section, the optimization objective, sensitivity factor, and a general purpose algorithm are introduced. In Section III, several design cases are evaluated. The degradation in the supply voltage and propagation delay before and after applying the proposed link breaking methodology is summarized. Additional topics related to evaluating and enhancing the link breaking methodology are discussed in Section IV. The conclusions are summarized in Section V.

II. LINK BREAKING METHODOLOGY

A link breaking methodology for determining which links should be removed, thereby shielding the sensitive circuits, is described in this section. This section is composed of three subsections. The sensitivity factor is introduced in Section II-A. In Section II-B, the objective of improving the worst case delay is described. A general purpose algorithm for the link breaking methodology is presented in Section II-C.

Algorithm 1 Pseudocode for link breaking methodology.

```
LINK-BREAKING
1. Determine voltage drops over power network
2. Calculate initial $delay_{ini}$ function based on (2)
3. Generate $x$ randomly perturbed systems
4. Determine voltage drops for $x$ systems
5. Calculate delay function based on (2) for $x$ systems
6. For every $x$ systems
7. Generate six different networks, where a link is broken at every direction
8. Determine new delay values, maintaining network with lowest delay
9. Goto 7, if improvement is achieved
10. Select system with lowest delay
11. If $delay_{ini} > delay$, $delay_{ini} ← delay$ and goto 3
```

A. Sensitivity Factor

The sensitivity factor describes the relative importance of a change in voltage on the performance of a circuit. A method to describe the sensitivity factor is to investigate the sensitivity of the supplied voltage on the performance (e.g., the propagation delay) of a particular circuit. The sensitivity factor in this case is [13]

$$s = \frac{\Delta delay(dj)}{(\Delta V/Vj)} \bigg|_{x = Vdd} = \frac{\Delta delay}{\Delta V} \cdot \frac{Vdd}{delay_{min}} \quad (1)$$

where $\Delta delay$ and $delay_{min}$ are, respectively, the change in the delay and the minimum delay of a circuit. The minimum delay is achieved assuming a full $Vdd$ at the power rail of the circuit. $\Delta V$ is the change in the supply voltage at the node supplied to the circuit. The sensitivity factor is dependent on the type of circuit.

B. Worst Case Delay

Each circuit within a network can be characterized as both an aggressor and a victim; therefore, each node of interest is associated with a matrix composed of two parameters $[i, j]$. Parameter $i$ is an aggressor-related parameter, and is equal to the load current sunk by the circuit. Parameter $s$ is related to the victim parameter, expressing the sensitivity of the circuit connected to the node. The objective is to enhance overall performance, such as minimize the worst case delay

$$delay_{worst} = \max (delay_1, delay_2, \ldots, delay_x) \quad (2)$$

where

$$delay_j = delay_{min} - \left\lbrack \left\lbrack \frac{Vj}{Vdd} \cdot \Delta V_j + 1 \right\rbrack \right\rbrack \quad (3)$$

$\Delta V_j$ is a change in the voltage at node $j$ due to the load currents and power network impedance. $delay_{min} - j$ is the minimum propagation delay of circuit $j$ while applying the maximum supply voltage $Vdd$. $s_j$ is the sensitivity factor of circuit $j$.

C. General Purpose Algorithm

Pseudocode of the link breaking algorithm for the proposed methodology is provided in Algorithm 1, with the objective of minimizing the worst case propagation delay. In line 1, the voltage drop across the power network is determined. Based on the voltage and sensitivity of the circuits, the initial value of the delay function $delay_{ini}$ is determined, as listed in line 2. Multiple power networks $x$ are generated, where each network is perturbed by removing a random link. In lines 4 and 5, the voltage drop and delay are determined for each of the perturbed networks. A search for a local minimum is evaluated for each perturbed system in lines 6–9. The network with the lowest delay is selected in line 10. The process is repeated until the delay cannot be further reduced.

To approach the global minimum, a larger number of perturbed systems $x$ is required. For the evaluated cases, $x$ is set equal to 10%
of the nodes within the system. A lower runtime is also achieved by evaluating those nodes directly connected to the victim or aggressor circuits.

III. Case Studies

Two study cases are presented in this section. The circuit is composed of nine blocks in each example. The sensitivity factor and critical delay of each block are assumed to be different. For the first case, block number 2 is assumed to sink significantly greater current, representing the case of a single dominant aggressor. In the second case, the sunk current is varied among all of the blocks, representing a general type of circuit. The design objective is to minimize the worst case propagation delay, as expressed in (2).

A mesh structured power distribution network with 20 × 20 number of nodes is considered. Four 1 V power supplies are connected at the center of the four edges (left, right, top, and bottom). The maximum permitted degradation in supply voltage is 0.3 V.

The supply voltage map before and after application of the link breaking methodology, as well as the resulting power network, are illustrated in Fig. 2. The current sunk before and after application of the methodology, sensitivity, propagation delay, and improvement in the supply voltage and propagation delay are listed in Table I.

In the first case [see Fig. 2(a) and (b)], the current sunk by the aggressor is significantly higher than the other circuit blocks. The highest degradation in supply voltage is within the aggressor circuit. The supply voltage, however, is greater (the voltage drop is lower) in those circuit blocks with a higher sensitivity and minimum delay, resulting in a reduction in the worst case delay and an increase in the maximum operating frequency. The increase in the supply voltage at block 1 is 5%, achieving 97% of the ideal power supply voltage and resulting in an improvement in the propagation delay of 18%. Note that the improvement in the delay is greater than the supply voltage because of the high sensitivity factor. After applying the link breaking methodology, blocks 1, 4, and 6 exhibit a similar worst case propagation delay, demonstrating the effectiveness of the proposed methodology.

In the second case [see Fig. 2(e) and (f)], the current is different among several blocks. After applying the link breaking methodology, the supply voltage at block 1 is increased by 5% and the maximum operating frequency is enhanced by 20%.

A multiple voltage domain methodology has been applied to both case studies for comparison with the link breaking methodology. In the multiple voltage domain methodology, the power distribution network is divided into four separate networks. The voltage variation map for multiple voltage domains is shown in Fig. 2(d) and (h). Based on these case studies, the maximum voltage drop occurs at blocks two and three, respectively, for the first and second case study. A comparison of the link breaking methodology with the multiple voltage domain methodology is also summarized in Table I. A 6% and 8% improvement in delay for these case studies is achieved by utilizing the link breaking methodology as compared with multiple voltage domains.

IV. Discussion

The voltage drop within a power distribution network is investigated for circuit blocks with different current levels and sensitivities. The minimum propagation delay, delay\textsubscript{min}, is maintained. A 20 × 20 mesh structured power distribution network with two power supplies and two current sources (one aggressor and one victim) is considered. The voltage improvement at the victim and degradation at the aggressor are illustrated, respectively, in Fig. 3(a) and (b). Note that by assigning a higher sensitivity to the victim circuit, the voltage drop on the power network at the victim is reduced. Simultaneously, the voltage drop at the aggressor is increased, but the aggressor is less sensitive to voltage variations. The tradeoff between reducing the voltage drop at the victim while increasing the voltage drop at the aggressor is an important aspect of the proposed link breaking methodology.

In the current version of the link breaking methodology, an optimization step is performed to reduce the DC noise (or worst
TABLE I
Sensitivity Factor, Sunk Current, Minimum Delay, Supply Voltage, and Propagation Delay Utilizing Uniform Grid, Link Breaking, and Multiple Voltage Domains Methodology for the Nine Circuit Blocks. The Improvement or Degradation Utilizing the Link Breaking Methodology in the Supply Voltage, Propagation Delay, and Maximum Operating Frequency Are Also Listed. Case 1 Represents the Case Where a Single Block Sinks Significantly Higher Current as Compared with the Other Blocks. In Case 2, the Sunk Current, Sensitivity Factor, and Delay Are Different for Various Blocks, Representing a General Design Case

<table>
<thead>
<tr>
<th>Block number</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>( f_{\text{max}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sensitivity factor (s)</td>
<td>5</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>1.3</td>
<td>3</td>
<td>1.2</td>
<td>4</td>
<td>——</td>
</tr>
<tr>
<td>Delay [ps] @ ( V_{dd} = 1V )</td>
<td>670</td>
<td>300</td>
<td>650</td>
<td>710</td>
<td>200</td>
<td>690</td>
<td>300</td>
<td>300</td>
<td>300</td>
<td>——</td>
</tr>
</tbody>
</table>

### Case 1 [see Fig. 2(a), (b), and (d)]

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Uniform grid [mV]</th>
<th>Link breaking [mV]</th>
<th>Multiple voltage domains [mV]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sunk current</td>
<td>924</td>
<td>850</td>
<td>924</td>
</tr>
<tr>
<td>Link breaking [ps]</td>
<td>973</td>
<td>702</td>
<td>861</td>
</tr>
<tr>
<td>Multiple voltage domains [mV]</td>
<td>955</td>
<td>784</td>
<td>843</td>
</tr>
<tr>
<td>Delay [ps]</td>
<td>988</td>
<td>369</td>
<td>748</td>
</tr>
<tr>
<td>Link breaking [ps]</td>
<td>829</td>
<td>422</td>
<td>807</td>
</tr>
<tr>
<td>Multiple voltage domains [ps]</td>
<td>887</td>
<td>393</td>
<td>824</td>
</tr>
<tr>
<td>Impr. versus uniform grid [%]</td>
<td>16.0</td>
<td>−15.0</td>
<td>−7.8</td>
</tr>
<tr>
<td>Impr. versus multiple voltage domains [%]</td>
<td>6.6</td>
<td>−7.5</td>
<td>2.0</td>
</tr>
</tbody>
</table>

### Case 2 [see Fig. 2(c), (f), and (h)]

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Uniform grid [mV]</th>
<th>Link breaking [mV]</th>
<th>Multiple voltage domains [mV]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sunk current</td>
<td>907</td>
<td>861</td>
<td>850</td>
</tr>
<tr>
<td>Link breaking [ps]</td>
<td>958</td>
<td>825</td>
<td>781</td>
</tr>
<tr>
<td>Multiple voltage domains [mV]</td>
<td>936</td>
<td>818</td>
<td>751</td>
</tr>
<tr>
<td>Delay [ps]</td>
<td>1050</td>
<td>366</td>
<td>800</td>
</tr>
<tr>
<td>Link breaking [ps]</td>
<td>870</td>
<td>378</td>
<td>847</td>
</tr>
<tr>
<td>Multiple voltage domains [ps]</td>
<td>947</td>
<td>380</td>
<td>868</td>
</tr>
<tr>
<td>Impr. versus uniform grid [%]</td>
<td>17.1</td>
<td>−3.2</td>
<td>−5.8</td>
</tr>
<tr>
<td>Impr. versus multiple voltage domains [%]</td>
<td>8.1</td>
<td>0.6</td>
<td>2.4</td>
</tr>
</tbody>
</table>

Fig. 3. Change in voltage drop for (a) victim and (b) aggressor circuits. The darker shade represents a greater reduction in the voltage drop at the victim and a small increase in the voltage drop at the aggressor.

Fig. 4. Decoupling capacitor is placed in close electrical proximity to the sensitive node (shown as a black dot) and is kept electrically distant from other nodes (all nodes to the left of the black dot). In this configuration, the majority of the charge from the decoupling capacitor is devoted to the sensitive node.

The proposed algorithm, depicted in Algorithm 1, is a general purpose algorithm not chosen with computational complexity in mind. Computational complexity can be reduced by evaluating only those nodes in the power distribution network directly connected to the victim and aggressor circuits, or clustering victim and aggressor nodes into groups. In those cases, where the number of nodes is low, the random walk approach [14] can be used, significantly reducing the computational complexity since the matrix inversion step is no longer needed.

In large scale networks, the computational complexity can be reduced by hierarchical partitioning or applying multigrid techniques [15]. In either case, the power network is smaller, optimized locally, and later combined. Note that the link breaking methodology can be applied at each stage, initially within a small portion of the power network and at each higher hierarchical level, only breaking the links at the intersection of the partitioned power network.

The link breaking methodology can also be applied at two separate stages. Initially, at the floorplanning stage, based on current consumption expectations and the impedance of the power distribution network, the majority of the links may be broken to improve performance. At the final stage of the design process, the link breaking...
methodology may again be applied to further refine the design of the power distribution network.

Decoupling capacitor allocation can also be integrated into the link breaking methodology, further improving power integrity. In Fig. 4, a decoupling capacitor is placed electrically close to a sensitive circuit and kept electrically distant from other circuits [16]. In this configuration, the majority of the charge from the decoupling capacitor is dedicated to the sensitive circuits. Including decoupling capacitor placement within this link breaking methodology or breaking the links while considering the placement of the decoupling capacitors can further optimize the overall power network.

V. Conclusion

The design of the power distribution network is an essential part of an IC design flow. The network is typically designed as a single network or multiple separate networks. The advantages of a single network are reduced network impedance and fewer routability constraints, while multiple separate networks have the advantage of lower noise coupling. The proposed link breaking methodology utilized a single network, disconnecting the links between the aggressive and sensitive circuits, thereby isolating the victim from the aggressor. This approach reduced the noise, while maintaining a low network impedance.

Sensitivity to changes in the supply voltage varies for different circuits. A smaller voltage drop is more important in long critical paths as compared with shorter, less critical logic paths. Voltage variations at the more sensitive circuits need to be reduced at the expense of increased voltage variations at the less sensitive circuits.

The proposed methodology is based on a mesh structured power distribution network. The aggressiveness and sensitivity of a circuit are considered during the link breaking process. The methodology is evaluated for several cases with a different number and magnitude of current and sensitivity factors. The objective for these cases is reduced worst case propagation delay by increasing the supply voltage at critical blocks with a high propagation delay. An average enhancement of 5% in power supply voltage at nodes with high sensitivity and high propagation delay is achieved, resulting in, on average, 96% of the ideal power supply voltage at these nodes. As a result, an average improvement of 16% in the maximum operating frequency is achieved when utilizing the proposed link breaking methodology. The link breaking methodology is also compared with a multiple voltage domain methodology, achieving an average 7% improvement in operating frequency.

REFERENCES