Thermal-Scheduling For Ultra Low Power Mobile Microprocessor

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Abstract

A thermal scheduling technique is proposed to minimize the performance/usage impact when thermal control mechanism is triggered. This technique uses on-chip I/O interface signal to classify the usage mode and thermal sensors to detect hot-spots within the microprocessor die. The thermal control and related voltage/frequency scaling mechanism to be implemented as the best for a given applications demanding performance and power conservation at runtime. There is a secondary pipeline segment within the core. It is architecturally simple with ultra low power implementation. This secondary pipeline segment has two main functions: 1.Ultra low power implementation for certain mobile usage modes (such as any where any time email connecting function); 2.Thermal relieve. When only low performance applications is running on the microprocessor, such as text email/message receiver mode, the segment of second pipeline is engaged. The primary complex out of order superscalar pipelines is either clock-gated or power gated or significant voltage scaling. The implementation arrangement is not only reduce the active power. It also decreases the leakage due to low operational temperature. Since the secondary pipeline consumes much less power, it will have a much lower temperature, and therefore, this implementation will provide a temporary thermal relieve to the core pipelines in additional to other power reduction techniques when the requested uage mode or thermal/power mechanism is triggered. This relief reduces energy loss due to leakage, prevents overheating to improve product reliability, and eases cost for thermal solutions. In the presentation, we compared an example of proposed implementation with two other thermal/power control techniques, namely dynamic clock disabling and dynamic frequency scaling. The example exhibits an 11.4% improvement in overall energy-performance metric with 4.6% increase in area.