

# The Design of Low-Latency Interfaces for Mixed-Timing Systems

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## Abstract

A critical challenge in designing large and complex digital systems is to gracefully support the use of heterogeneous components. There are two fundamental issues: (i) interfacing systems operating under different timing assumptions, and (ii) handling long communication delays between these systems. This talk addresses both of these issues.

In particular, a new family of low-latency FIFO's is introduced that can robustly interface systems operating at different speeds. The connected systems can be either synchronous or asynchronous. The new interface circuits are then modified to work between systems with very long interconnection delays, by migrating a single-clock solution by Carloni et al. [1] (for so-called "latency-insensitive" protocols) to mixed-timing domains. The designs can be made arbitrarily robust with regard to metastability and interface operating speeds. Initial simulations for both latency and throughput are promising. (For a detailed technical presentation, see [2].)

## References

- [1] L. Carloni, K. McMillan, A. Saldanha, A. Sangiovanni-Vincentelli, "A Methodology for Correct-by-Construction Latency Insensitive Design", ICCAD'99.
- [2] T. Chelcea, S. Nowick, "Robust Interfaces for Mixed-Timing Systems with Application to Latency-Insensitive Protocols", in Proceedings of the IEEE/ACM Design Automation Conference, pp. 21-26, Las Vegas, NV (June 2001).

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