

## Invited Presentation

### Low Power Locally Asynchronous Interlocked Pipelined CMOS Clock Circuits Operating at 3.3-4.5 GHz:

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**Abstract:** While it is possible to reduce processor clocking and latch power by adopting a globally asynchronous and locally synchronous approach, that approach tends to make the machine appear asynchronous at its highest level of description. In developing the circuitry of IPCMOS, we have taken rather the reverse approach, in which a globally synchronous processor is provided with locally asynchronous structures for executing operations. These locally asynchronous components can be interfaced to the synchronous environment in a manner that makes the entire design appear synchronous, while significantly reducing the latch count driven by the synchronous clocks. In this paper IPCMOS clock circuits suitable for high frequency and low power operation are described. In IPCMOS (as in other asynchronous techniques) the reduced power results from enabling the local clocks only when there is an operation to perform. In addition, the latches controlled by the IPCMOS clocks can be simple single stage latches because the locally generated clocks driving adjacent stages are not enabled simultaneously. The combination of enabling the clocks only when there is an operation to perform and the simple latch can lower power by a factor of 5x to 10x in many pipeline applications. In IPCMOS the staggered local clocks also result in a significant reduction of dynamic  $L di/dt$  noise. In addition to the locally generated interlocked clocks and the single stage latch, unique circuits that combine the function of a static NOR and an input switch are key to achieving high performance and minimizing the overhead in the interlocking. In a 0.18 $\mu$ m bulk CMOS technology these circuits drive a path through a typical 64b multiplier stage at 3.3 - 4.5 GHz on an experimental chip.