

# Keynote Presentation

## High Performance with Manageable Complexity: The IBM POWER4<sup>TM</sup> Experience

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**Abstract:** The IBM POWER series processors (first available in 1990 through the initial RS/6000<sup>TM</sup> workstation) started out as a RISC “braniac.” Hardware complexity reduction was an issue even then, but it was addressed mainly by inventing a simpler, load-store instruction set paired with smart optimizing compiler technology. The microarchitecture definition for the first POWER and PowerPC super scalars, however, continued on the braniac path, with relatively lower frequencies (short pipelines), increasing issue widths, ever-greater degrees of speculation and overlapped processing of instructions. This “microarchitecture-compiler” centric definition approach, did not scale well in terms of delivered performance beyond the mid-90’s, however, since aggressive circuit design methods and tools were not invested into in the context of rather conservative frequency targets. Also, since the ISA had to remain practically unchanged, and compiler-derived improvements dwindled, there was a tendency to increase microarchitectural complexity in order to meet net performance targets. In view of the increasing gap between processor and memory speeds, however, it became clear that remaining on the strict braniac path was not going to be “complexity-effective.” As such, beyond the POWER3 microprocessor a more balanced approach was adopted, with a conscious shift toward the “speed demon” philosophy and a more “system performance” viewpoint in defining the chip-level microarchitecture. (Concurrently with the POWER3 family designs, IBM also developed the RS64-series 64-bit PowerPC<sup>TM</sup> microprocessors that have demonstrated scalability in performance through simpler microarchitectures with hardware multithreading to alleviate the memory latency approach).

In this talk, we provide an overview of the POWER4 system microarchitecture: with an explanation of how the net performance goals were met with manageable complexity and without schedule delays. The POWER4 design was initially introduced at processor frequencies of 1.1 GHz and 1.3 GHz, surpassing all other 64-bit microprocessors in key performance benchmarks. We begin with a view of the initial design philosophy in the context of the background stated in the previous paragraph. Later, after we describe the microarchitecture we re-examine the issue of complexity-effectiveness as we compare the POWER4 approach with the prior POWER3-series and RS64-series microprocessors. We will examine the effect of this design constraint on future processor microarchitectures.