

# Using a Performance Model to Estimate Core Clock-gating Power Savings

*Workshop of Complexity-Effective Design  
In Conjunction with ISCA 2002*

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# Agenda

- **Introduction**
- **Complexity Issues**
- **Modeling Methodology**
- **Clock Gating Events Selection Criteria**
- **Sample Clock Gating Events**
- **Performance Model**
- **Conclusions and Future Work**

# Introduction

- **Microprocessor power increase raises chip cooling cost and Introduces reliability concerns.**
- **70% of the Power4 chip power (115W) is consumed in the clocking elements [C. Anderson, et al., ISSCC 2001].**
- **Clock gating ... but:**
  - ▲ **Quantifying power savings.**
  - ▲ **Study power swings.**
  - ▲ **Steering complexity vs. power savings decision.**

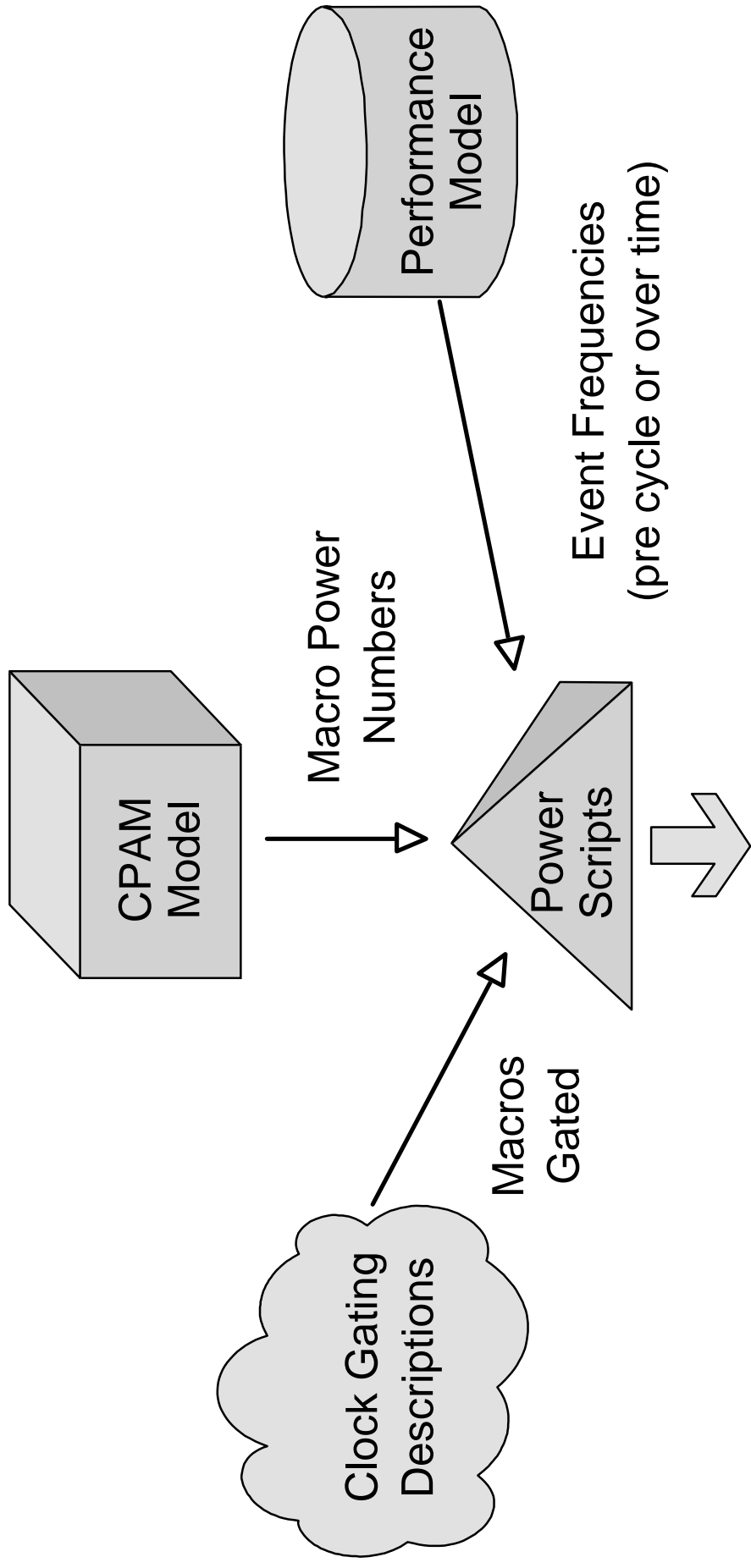
# Complexity Issues

- **So much data at many design levels.**
    - ▲ **Macro level power consumption.**
      - **Macros input switching factors.**
      - **Internal node switching.**
    - ▲ **Circuit level clock gating options.**
    - ▲ **Architectural level clock gating events (conditions).**
  - **Clock gating effect on cycle-to-cycle power swings.**
    - ▲ **Noise, decoupling cap, and area tradeoff.**
  - **Does a clock gating event pull its weight?**
    - ▲ **Design complexity, timing, and verification.**
- Vs. power saving.**

# Power Modeling Methodology

- **Candidate clock gating events are presented by circuits designers.**
  - ▲ **Circuit signals and associated macros list pairs.**
  - ▲ **Percentages of macros power saving.**
  - ▲ **Clock gating events are subject to selection criteria.**
- **CPAM tool provides macros power numbers.**
  - ▲ **Detailed analysis of all macros.**
  - ▲ **Decoupling, wire, intrinsic, and parasitic cap.**
  - ▲ **Random input vectors with user-specified SF.**
- **Performance simulator provides estimation of events occurrence.**

# Power Modeling Methodology Cont.,



Total power saved over whole run and for each cycle, per unit and for the core

# Power Simulation Modes

- **Average power for the overall simulation period.**
  - ▲ **Achieved preset power savings goal?**
- **Dynamic averages over specific time periods.**
  - ▲ **Dynamic behavior of unit powers, chip power, and events patterns.**
- **Cycle-to-cycle power swing.**
  - ▲ **Noise induced if too many macros are gated/activated in one cycle.**
  - ▲ **Define decoupling cap. values and locations.**

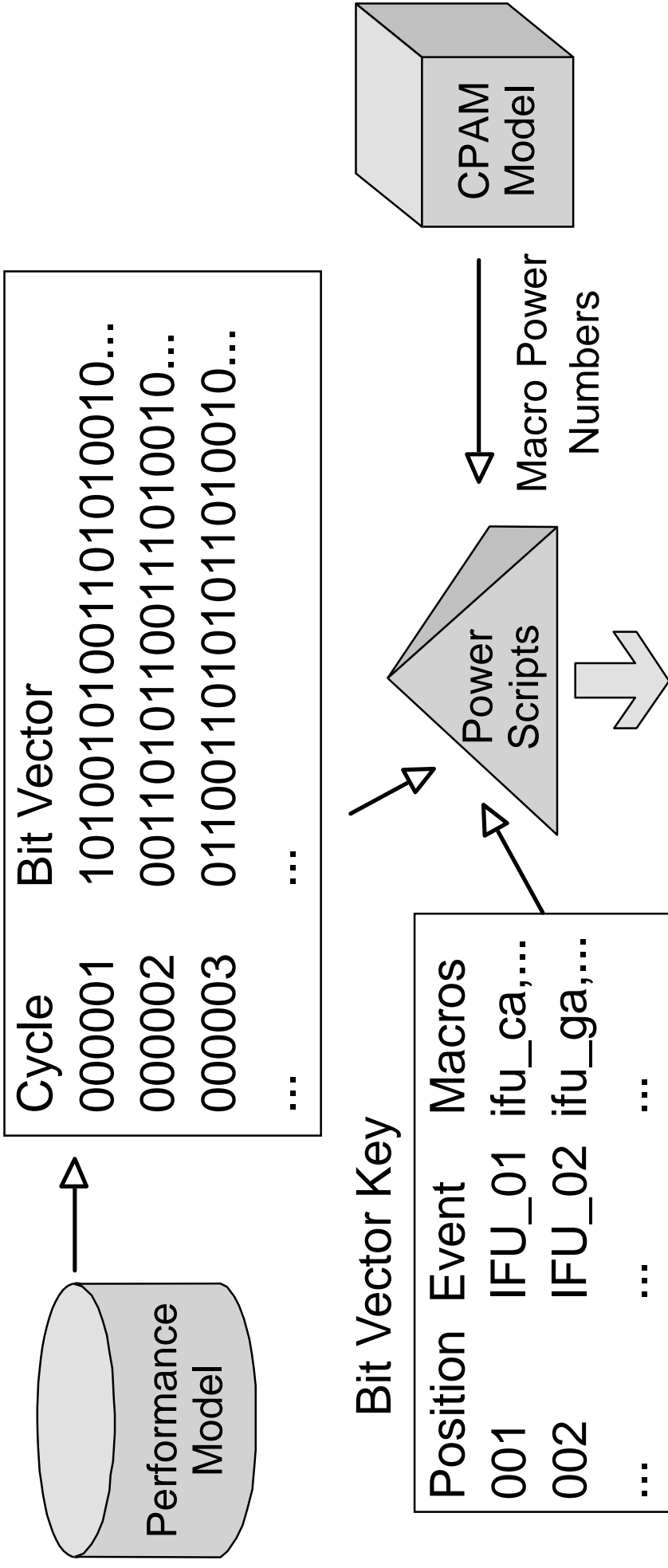
# Power Swing Modeling Methodology

- **Store the state of all events in every cycle for a million cycles.**
  - ▲ **Bit vector and macros key map.**
- **Produce short sub-trace (10 cycles) if a power swing threshold is hit.**
- **Produce histograms for each unit as well as the whole core/chip.**
  - ▲ **Additional decoupling capacitors very close to trouble spots.**
  - ▲ **Helps to perform power saving vs. area and noise tradeoff.**

# Power Swing Modeling Methodology

## Cont.,

Million cycle trace of the state of all events per cycle



Histograms of the each cycles power swings for the core and each unit.

# Clock-gating Events Selection Criteria

- **Frequent.**
- **Considerable power saving.**
- **Select coarse granularity.**
- **Simple.**
- **Limit small number of event per unit.**
- **Shallow depth of gated macros.**
- **Not too many fragmented events.**
- **No new critical paths.**

# Clock-gating Events Examples

*Event*

*Clock gated structure(s)*

ICache miss IERAT miss & IFB full	ICache & directory IERAT Branch prediction array & logic
Not Microcode Inst.	Microcode ROM
L2 not returning data	Predecode PLA
Queue entry/section not written	Queue entry/section

# Performance Simulation Model

- **Cycle accurate .**
- **Verified against VHDL.**
- **Trace driven (no data values).**
- **Varying degrees of speculation.**
- **Advantages to using performance model:**
  - ▲ **The power model can be ported to different architectures/simulators easily.**
  - ▲ **Modular design, easily modified.**
  - ▲ **Early rough estimation for power savings.**
  - ▲ **Highly parameterized.**
  - ▲ **Evaluate different power savings techniques.**
    - **Throttling, adaptive queue sizing, ... etc.**

# **Drawbacks of Our Current Performance Model**

- **Accuracy of power estimation.**
- **Data values not in trace => no switching factors.**
  - ▲ **Not a methodology limitation.**
  - ▲ **Initial estimate, can be followed by more analysis once the design is further along.**
- **Very large output file size.**
- **Step-power not Ldi/dt.**

# Conclusions and Future Work

- **By integrating data from circuit, macro, and architectural levels, power savings projections, design tradeoffs, and cycle-to-cycle power swings estimates are modeled.**
- **Future work:**
  - ▲ **Integrating power model into performance model.**
  - ▲ **Integrating power delivery model.**
  - ▲ **Improving power modeling => account for switching activity.**