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# Power Estimation of a C algorithm on a VLIW Processor

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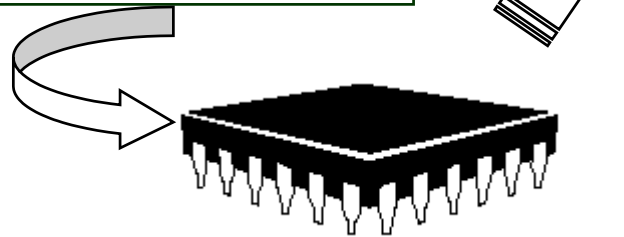
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# Context

## C-level estimation **WITHOUT** compilation

```
test1(int IU, int JU, int KU)
{
    int i, j, k;
    for(i=0; i<IU; i++)
        for(j=0; j<JU; j++) {
            for(k=8; k<KU; k++)
                A[k] = A[k-8];
            B[i][j] = B[i+1][j] + A[i];
        }
    for(i=0; i<IU; i++)
        for(j=0; j<JU; j++)
            B[i][j] = B[i][j] +
B[i+1][j];
}
```

**P ?**



**Complete power model**

# Power Estimation

## Gate level estimation:

- very accurate but long simulation time
- RTL description needed

RTL description not available

## Instruction Level P. A.

- accurate
- limited for VLIW processor
  - compiler dependent
  - memories and pipeline stalls not taken into account

## Functional Level P. A.

- accurate & fast
- based on architecture analysis
  - compiler independent
  - memories and pipeline stalls taken into account

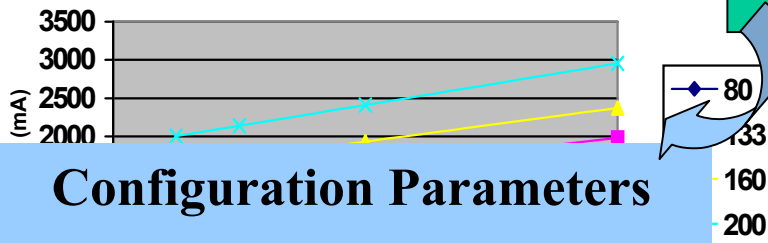
# Methodology: Model Definition

## Algorithmic parameters

Parallelism, Processing units

Cache miss, Pipeline Stalls...

Consumption in mapped mode



## Configuration Parameters

Frequency, Memory Mode...

0 0,25 0,5 0,75 1

Parallelism rate (%)

Parameters

Power Model

$$P = 4 \alpha + 1$$

Processor

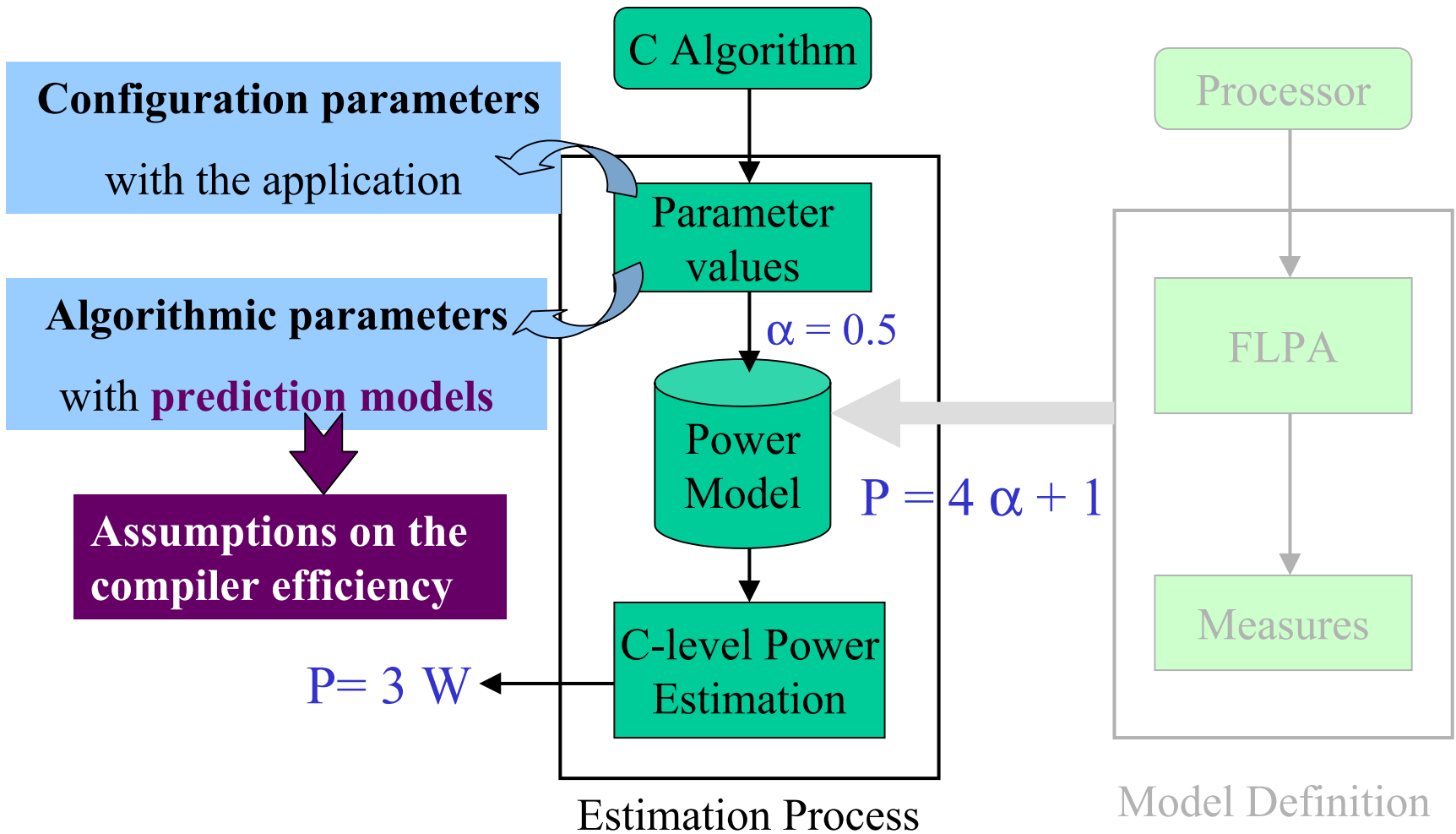
FLPA

Measures

$\alpha$

Model Definition

# Methodology: Estimation Process



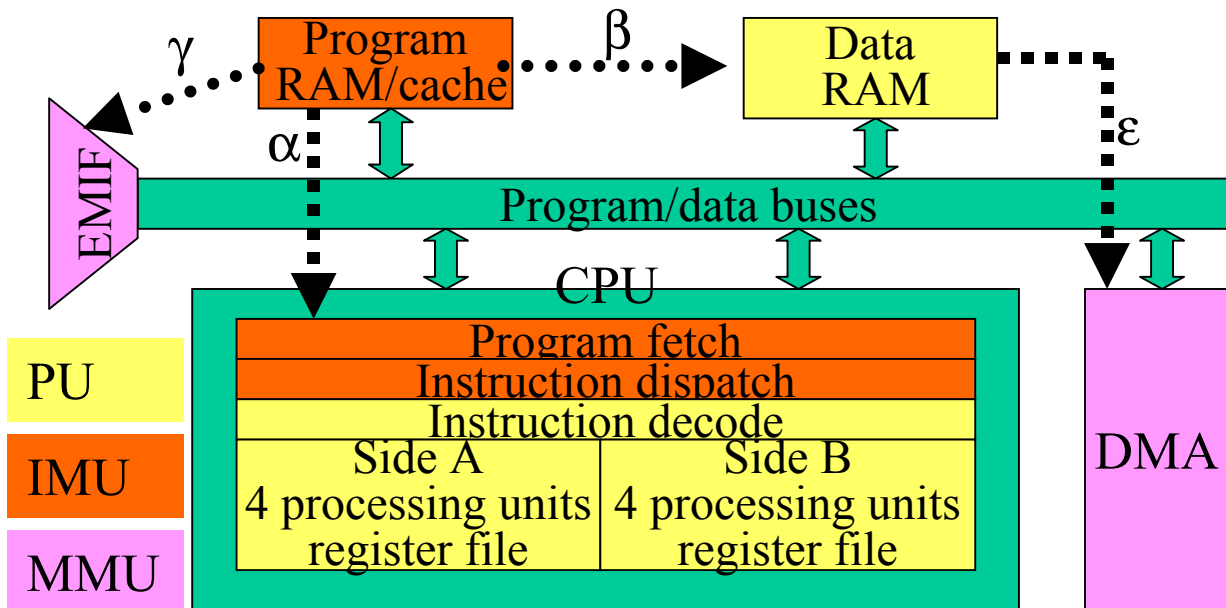
# TI C6x: Model Definition

## TI TMS320C6201: VLIW processor

*up to 8 instructions in parallel, deep pipeline (up to 11 stages),  
4 memory modes: mapped, bypass, cache and freeze*

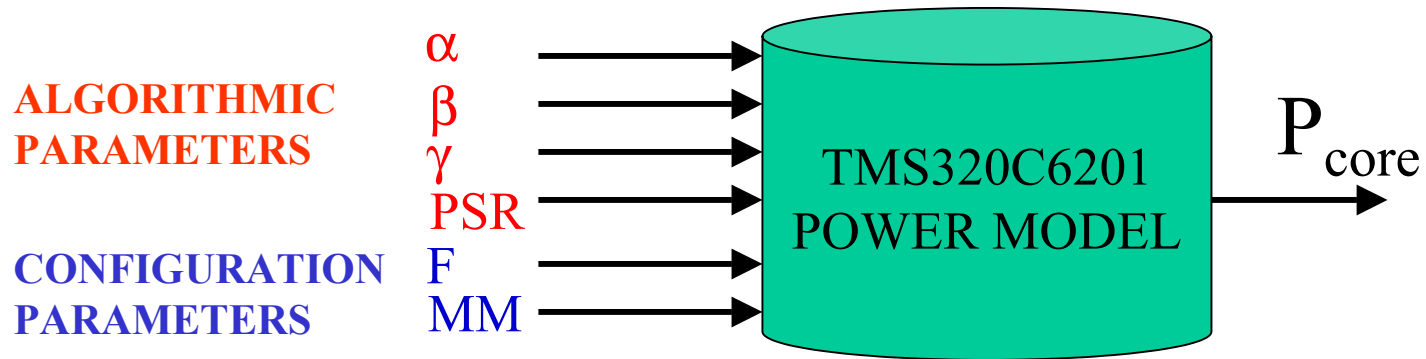


## FLPA: Functional-Level Power Analysis



$\alpha$  : parallelism rate  
 $\beta$  : number of processing units  
 $\gamma$  : cache miss rate  
 PSR : pipeline stall rate  
 $F$  : clock frequency  
 MM : memory mode

# TI C6x: Power Model



Power consumption rule in **mapped mode**

$$P_{core} = V_{DD} * ([a\beta(1-PSR) + b_m] F + \alpha(1-PSR) [a_m F + c_m] + d_m)$$

measurements:  $a=0.64$ ,  $a_m=5.21$ ,  $b_m=4.19$ ,  $c_m=42.401$ , and  $d_m=7.6$

# Parameters extraction

X=a+b;

Y=c+d;

*for (i=0;i<10;i++)*

*y[i]=c[i]\*d[i+1];*

Z=a+d;

*for (j=0;j<50;j++)*

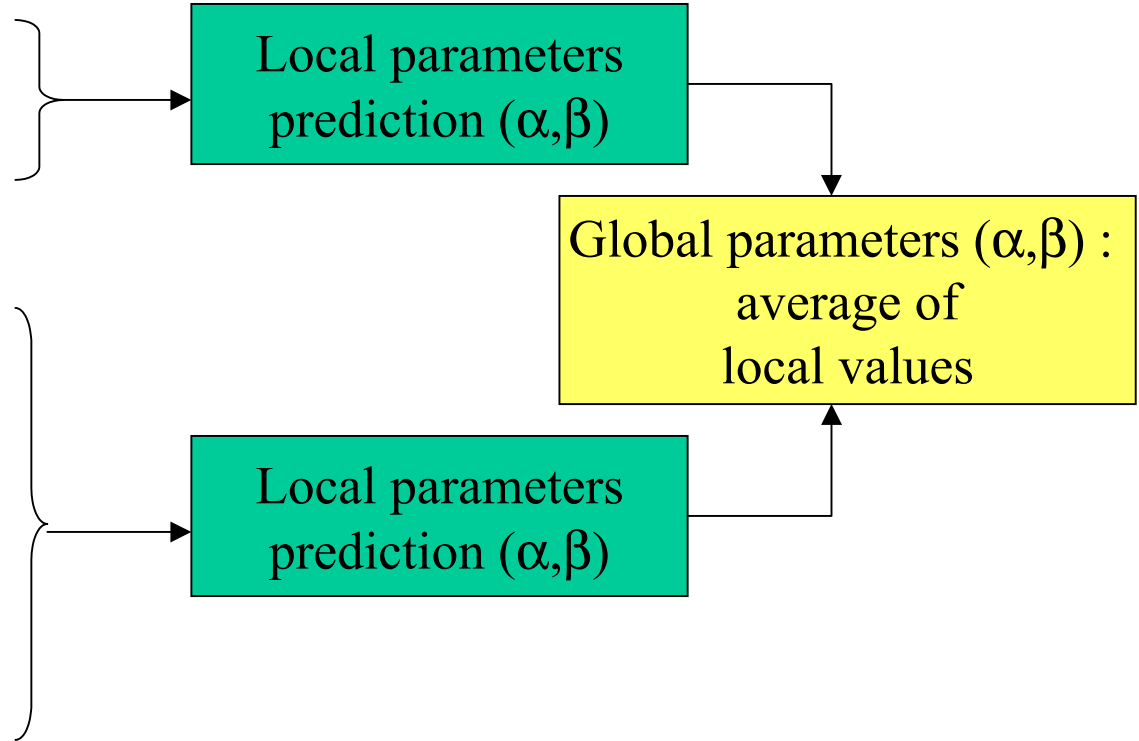
*{*

*for(k=0;k<32;k++)*

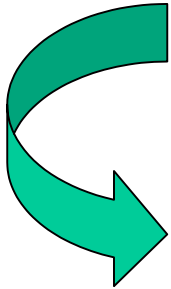
*tab[k]=h[k-1]+l[k+1]*

*}*

Loop nests analysis



# Parameters extraction



For (i=0; i<512; i++) Y= x[i]\*(h[i] + h[i+1] + h[i-1]) + y;

Loop body: 8 instructions = 4 LD, 4 OP

NFP = 1; NPU = 8

$$\alpha = \frac{NFP}{NEP} \leq 1 ; \beta = \frac{1 \text{ NPU}}{8 \text{ NEP}} \leq 1$$

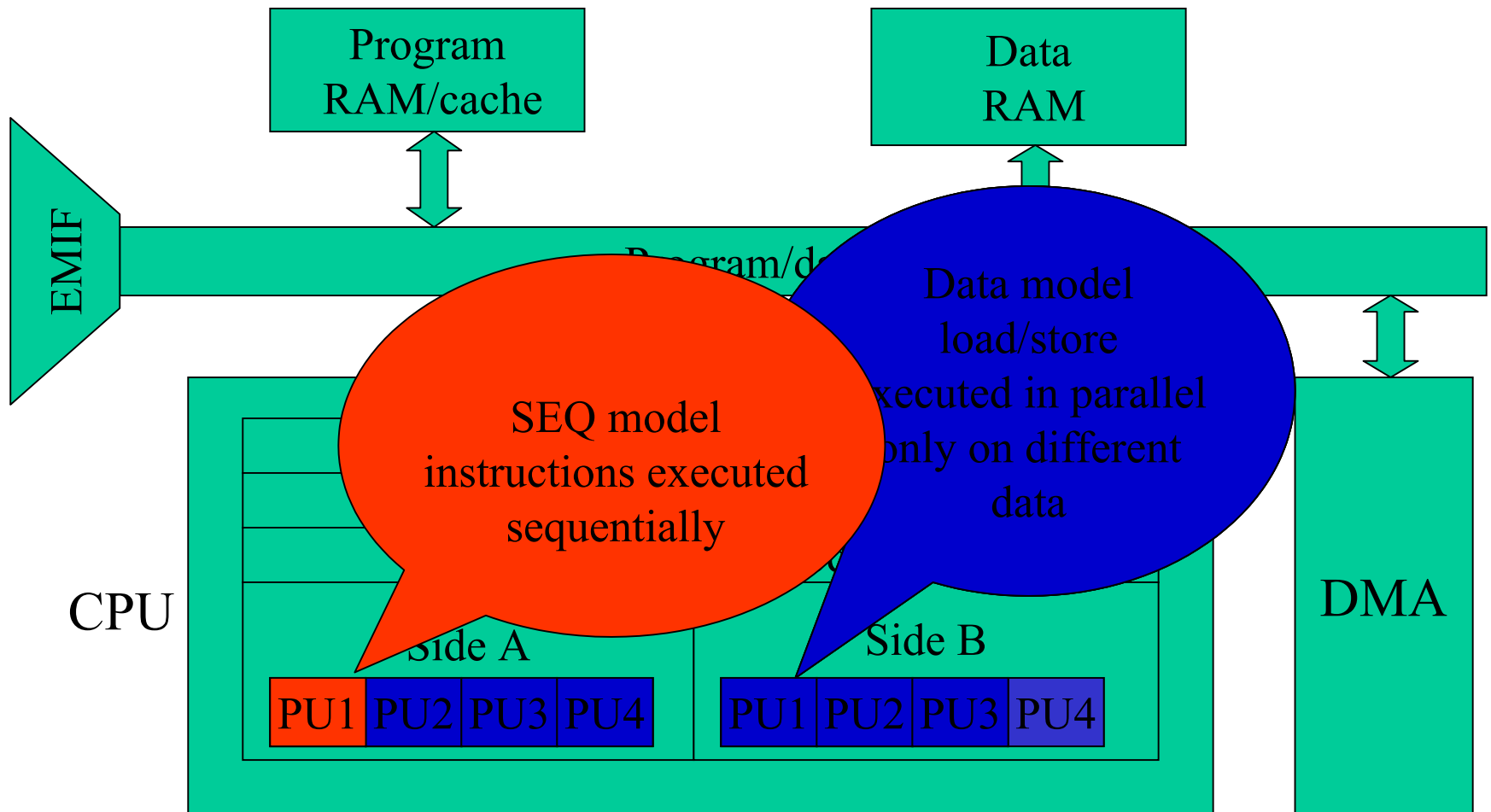
NFP: Number of Fetch Packets

NPU: Number of Processing Units

NEP: Number of Execution Packets

PREDICTION MODEL	EP1	EP2	EP3	EP4	$\alpha, \beta$
SEQ	8 EP				0.125
MAX	2 LD	2 LD 4 OP	-	-	0.5
MIN	1 LD	1 LD	1 LD	1 LD 4 OP	0.25
DATA	2 LD	1 LD	1 LD 4 OP	-	0.33

# Prediction models



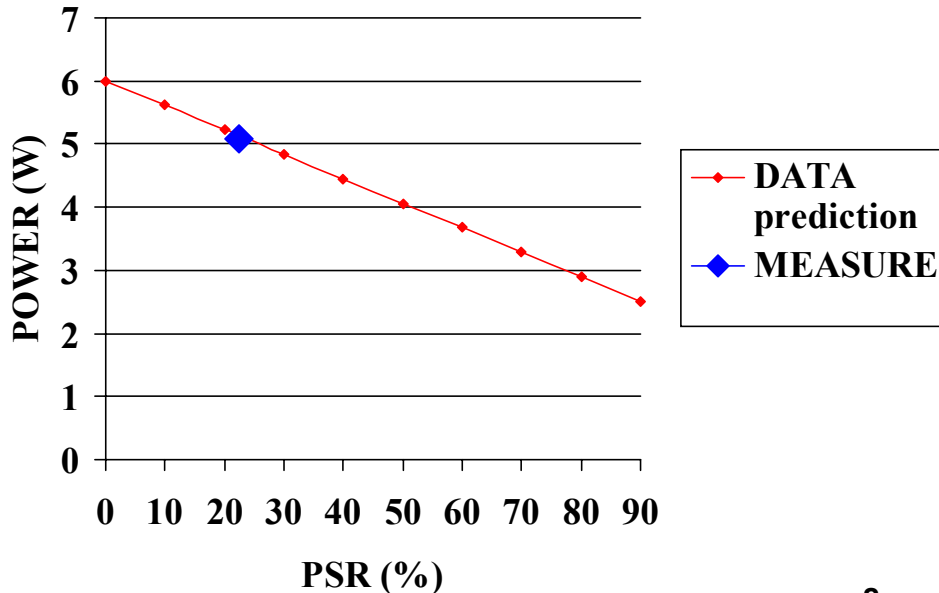
# Results

Algorithm			Measures	Estimation vs Measures (%)			
Application	MM	INT/EXT		SEQ	MAX	MIN	DATA
FIR	MM <sub>M</sub>	INT	4.5	-39%	+5%	-33%	+5%
FFT	MM <sub>M</sub>	INT	2.65	-11%	+12%	-3%	-2.6%
LMS	MM <sub>B</sub>	INT	4.97	+1%	+3%	+2%	+3%
LMS	MM <sub>C</sub>	INT	5.67	-55%	+5.8%	-16%	+5.8%
DWT 64*64	MM <sub>M</sub>	INT	3.75	-25%	+13%	-13%	-5.9%
DWT 64*64	MM <sub>M</sub>	EXT	2.55	-10%	+3%	-5.9%	-3.5%
DWT 512*512	MM <sub>M</sub>	EXT	2.55	-11%	+2.4%	-7%	-3.9%
EFR vocoder	MM <sub>M</sub>	INT	5.08	-50%	+11%	-24%	+1%
MPEG decoder	MM <sub>M</sub>	INT	5.82	-54%	+9.6%	-32%	-8%
Average error				32%	7.8%	17%	4.8%

- Estimation vs Measures < 8%
- Minimum and maximum bounds provided

# Consumption "maps"

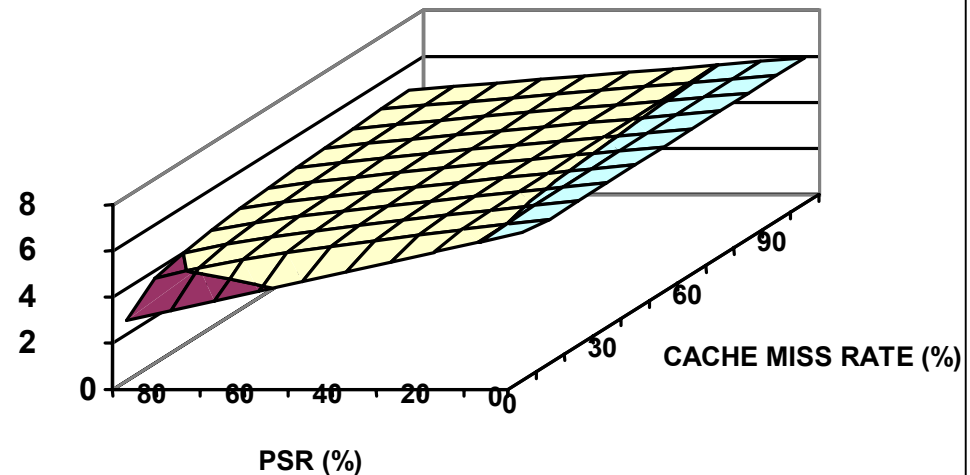
- Consumption maps for the EFR Vocoder



*In mapped mode*

POWER (W)

*In cache mode*



# PSR estimation

- $PSR = NPS / NTC$ 
  - NPS: number of cycles where the pipeline is stalled
  - NTC: total number of cycles
- $NPS = NPS\tau + NPSbc + NPS\gamma$ 
  - $NPS\tau$ : external data access - NEXT - Data Mapping (C-level)
  - $NPSbc$ : internal data bank conflict - NCONFLICT - Data Mapping (C-level)
  - $NPS\gamma$ : program cache misses - NFRAME - Compilation (A-level)

# Complexity reduction

- Only a portion of the code is to be studied
- Optimization effort can be focussed

Application	# of code lines		# of lines studied	
	C	ASM	Number	%C
FFT	77	408	10	13
LMS	30	408	4	13.3
DWT 64*64	46	714	17	37
EFR	118	1323	37	31.2
MPEG	2267	8488	30	1.3

# Conclusion

- Original and general approach validated on a VLIW DSP architecture
- Estimation of minimum and maximum bounds of an algorithm power consumption
- Fast and accurate power estimation at the C-level (error max = 8%)
- Refining at the assembly level (error max = 3%)
  - but compilation is needed then

# Conclusion

- Co-design HW/SW, SOC
- High level abstraction decision
  - no compilation
  - no physical measurements
  - no development tools and evaluation boards
- Fast feedback on software performances
  - hot spots
  - pieces of code not suitable for compilation yet
- Complexity reduction

# Current and Future works

- Development of an automatic tool in progress (available on-line before 2003)
- Extension of the power model library in progress (TI C55, ARM7)
- Execution time estimation for energy consumption
- Generic model for external memories