4-bit Pipelined Carry Select Adder Design Report

Alok Garg

December 09, 2004
1 Abstract

Design, layout and Performance evaluation of 4-bit pipelined carry-select adder is presented in this design report. The pipelined adder presented here consists of two stage of pipeline. The input setup ($T_{setup}$) and hold ($T_{hold}$) timings of the adder are 78ps and 0ps respectively. The clock to out delay ($t_{clk\rightarrow Out}$) at the output of the full-bit adder consists of $t_{clk\rightarrow Q}$ delay of flip-flop and propagation delay ($t_p$) of 2-bit multiplexer. The measured worst case delay is 340 ps. The design is validated for functionality, performance and power. The average power utilization is 0.441mW at 1GHz frequency. The design is validated to be working till 1.43GHz of operations. Hand-layout of the design is very optimized for area. The rectangular dimensions of the layout are 50.80μ × 39.29μ, with total area of 1995μ².

2 Introduction

Design of multi-bit full adders consists of two parts.

1. Full adder architecture: Carry-chain forms the critical path in any full-adder circuit. Various architectures has been evolved to optimize the carry chain path. Widely used adder architectures are: Ripple Carry Adder, Carry Skip Adder, Carry Select Adder, Square Root Carry Select Adder and Parallel Prefix Adders. These adder architectures vary in performance and power consumption. Few are good for performance and others are good for low power. In the current 4-bit adder design project, carry-select adder is used as the base architectures. This type of adder is normally used for high performance designs, where power is not a issue.

2. 1-bit Full adder carry logic design: Various design methodologies like static CMOS, CPL, TG or domino logic can be used for full adder design. Issues here are fast generation carry output, that can be used by the next stage as soon as possible.

The architectural Block diagram of the 4-bit Carry-Select adder is shown in Figure 1. This design leverages the benefits of carry select adder, by performing all the computations in one clock cycle, and proper computation can be selected from the lower bit carry out in the next pipeline stage. Since the delays of the MUX is typically very small, additional combinatorial logic
can be added after MUX within the next stage pipeline. Hence virtually allowing the 4-bit additions in less than $2 \times t$ time, where $t$ is the propagation delay of 2-bit adder.

Since we have already fixed the architecture of 4-bit carry-select adder, the design of 2-bit full adders is very critical for performance and minimum area requirements of the complete design. The design of 2-bit adder can also be divided into two components, design of 1-bit adder and design of carry-chain for the same.

## 3 Methodology

Various design options for 2-bit adder are explored in the analytical section. Options for the implementation of 1-bit full adder are:

1. XOR FA (TG based architecture).
2. CPL FA (CPL based architecture).
3. Delay Balanced FA.
4. Mirror Adder (Static CMOS based architecture).

Options for the design of carry chain are:

1. Ripple Carry Adder (RCA).
2. RCA with inversion Property.
3. Fast carry chain.
4. Manchester Carry Chain.
5. Carry-Skip Adder.

The rest of the document is divided as follows: Section 4 gives the analytical study of above discussed options. Here complete design is discussed to optimize the 2-bit adder for high performance and minimum area based on options available. In Section 5 Simulations are done a adder design and results are analyzed. This section also describes the experimental strategy followed. Section 6 discuss the layout design and verification of 4-bit adder. Section 7 Characterizes the 4-bit adder from simulation results. Section ?? discuss applications of the 4-bit adder presented in this report. Section 9 discuss further improvements and conclusions.

4 Analytical Study

As has been discussed earlier, 2-bit adder can be analyzed in two parts,

1. Carry Chain Design.
2. 1-bit Full adder design.

It is preferable to discuss first the selection of carry select design, based on which the 1-bit full adder design can be optimized keeping in mind the global architecture of 4-bit adder.
4.1 Carry Chain Design

1. Ripple Carry Adder (RCA).
2. RCA with inversion Property (RCAI).
3. Fast carry chain (FCC).
4. Manchester Carry Chain (MCC).
5. Carry-Skip Adder (CSkA).

Following table discuss in brief the properties of various carry chain design for 2-bit adder. Various issues (in the design of carry-chain) discussed in the table are:

1. Worst Case Delay: Worst case carry-chain delay is most critical for the performance of adder circuits. Here this worst case delay has been discussed with respect to 2-bit error.

2. Design Complexity: Design Complexity and worst case delays are inversely proportional. With the decrease in worst case delay, design complexity increases. And may be it does not make any sense for small adders.
<table>
<thead>
<tr>
<th>Type</th>
<th>Design Complexity</th>
<th>Worst Delay (n)</th>
<th>Worst Delay (2)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>RCA</td>
<td>Simple</td>
<td>O(n)</td>
<td>2</td>
<td>Simple design, best suited for small designs.</td>
</tr>
<tr>
<td>RCAI</td>
<td>Simple</td>
<td>O(n)</td>
<td>2</td>
<td>Better than simple RCA. Remove buffer delays.</td>
</tr>
<tr>
<td>FCC</td>
<td>Complex</td>
<td>log(n)</td>
<td>1</td>
<td>Very complex, large area and power requirements.</td>
</tr>
<tr>
<td>MCC</td>
<td>Avg Complex</td>
<td>O(n)</td>
<td>2</td>
<td>Clock based carry generation. Not good for current design.</td>
</tr>
<tr>
<td>CSkA</td>
<td>Avg Complex</td>
<td>O(√n)</td>
<td>1.44</td>
<td>Shortens the most critical path. May not make sense for 2-bit. But is good for large values of n.</td>
</tr>
</tbody>
</table>

From the above discussion, it seems that RCAI is best suited for 2-bit adder. Next designing with RCAI is discussed.

### 4.2 2-bit Adder design for RCAI

Block diagram for ripple carry adder with inversion property is shown in Figure 2 and Figure 3. As it appears from the block diagrams, 4 different type of 1-bit adders are needed to completely optimize the design for area. Next section talks about logic type selection for these adder designs.

### 4.3 1-bit full adder design

For simplification purposes, only one type of logic is used for design of all the four 1-bit adders. The type of logic styles that are discussed here are:
Figure 2: Block Diagram of 2-bit Ripple Carry Adder, with inversion property.

Figure 3: Block Diagram of Stage-1, 1-bit adder. (a) Stage-1 for 2-bit carry-select adder with carry input as '0'. (b) Stage-1 for 2-bit carry-select adder with carry input as '1'. (c) Stage-1 for 2-bit carry-select adder with carry input.
1. XOR FA (TG based architecture).

2. CPL FA (CPL based architecture).

3. Delay Balanced FA (DBFA).

4. Mirror Adder (Static CMOS based architecture) (M Adder).

Following parameters of all the logic styles has been discussed and analyzed.

1. Area (equivalent transistor count). For area calculation, each transistor is converted to equivalent minimum size transistor.

2. Length of critical path ($N_{crit}$). This is calculated in terms of number of transistors to be crossed from input, before signal reaches the output.

Following table provides the 1-bit Full adder comparative study. In the table, Time is in terms of delay through single transistor and Area is in terms of minimum size transistor count.
<table>
<thead>
<tr>
<th>FF Type</th>
<th>Area</th>
<th>Time</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>XOR FA</td>
<td>38</td>
<td>4</td>
<td>Fast, small in size, TG based, Easy to implement inversion properties without extra logic, few sizing issues.</td>
</tr>
<tr>
<td>CPL FA</td>
<td>55</td>
<td>4</td>
<td>Threshold drop problem, Easy to implement inversion logic (Complementary outputs), reduced noise margins.</td>
</tr>
<tr>
<td>DBFA</td>
<td>55</td>
<td>4</td>
<td>Identical delays for carry and sum, Requires good voltage swing, difficult to implement inversion property.</td>
</tr>
<tr>
<td>M Adder</td>
<td>111</td>
<td>3</td>
<td>Big in size, Sizing issues, inverted outputs only</td>
</tr>
</tbody>
</table>

After analyzing above table, simulations are done using XOR FA (TG based architecture). It seems to be most promising among all other architectures based on area. Performance is almost same for all logic styles. I would like to do simulations for Delay Balanced FA also, but due to time shortage, not able to finish it on time.

1-bit adders shown in Figure 4, 5, 6 and 7 are optimally designed using XOR FA (TG based architecture logic).

### 4.4 2 to 1 MUX

TG based $2 \rightarrow 1$ Mux is chosen for implementation because of it’s low area requirements. Since the output of the TG MUX has to be buffered, inverter chain of two minimum size inverters is used for buffering the outputs of Mux.
Figure 4: Stage-1 Full adder with carry input.

Figure 5: Stage-1 Full adder with carry input = 0.

Figure 6: Stage-1 Full adder with carry input = 1.
5 Schematic Simulations

Schematic diagrams of all the four circuits discussed in previous section are shown on the next page.

5.1 1-bit Stage-1 Full adder with carry input simulations

Waveform diagrams of 1-bit Stage-1 Full adder with carry input schematic simulations are shown on the next page. Table below, summarize the simulation results for this adder.

<table>
<thead>
<tr>
<th>Timing Parameter</th>
<th>Min Value</th>
<th>Max Value</th>
<th>Typical</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{p,L\rightarrow H}$</td>
<td>223</td>
<td>270</td>
<td>270</td>
<td>ps</td>
</tr>
<tr>
<td>$T_{p,H\rightarrow L}$</td>
<td>260</td>
<td>303</td>
<td>303</td>
<td>ps</td>
</tr>
<tr>
<td>Power (500MHz)</td>
<td>-</td>
<td>-</td>
<td>0.043</td>
<td>mW</td>
</tr>
<tr>
<td>$T_{rise}$</td>
<td>136</td>
<td>136</td>
<td>136</td>
<td>ps</td>
</tr>
<tr>
<td>$T_{fall}$</td>
<td>135</td>
<td>135</td>
<td>135</td>
<td>ps</td>
</tr>
</tbody>
</table>

5.2 Complete Design

The specifications of the 4-bit Adder test circuit is as follows:

1. Load Capacitance = 10 fF.
2. Clock Frequency = 500 MHz at 50% duty ratio.

3. Clock Rise Time = 100 ps.

4. Clock Fall Time = 100 ps.

5. Input Rise Time = 200 ps.

6. Input Fall Time = 200 ps.

Waveforms showing functional verification of schematic is also attached with schematic diagram. Please note that 4-bit input 'B' remains equal to input 'A' in all the waveforms. Hence is not shown in waveform diagrams. Table below, summarize the simulation results for 4-bit full adder.

<table>
<thead>
<tr>
<th>Timing Parameter</th>
<th>Min Value</th>
<th>Max Value</th>
<th>Typical</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>(T_{\text{clk}}\rightarrow\text{out,L}\rightarrow\text{H})</td>
<td>225</td>
<td>320</td>
<td>320</td>
<td>ps</td>
</tr>
<tr>
<td>(T_{\text{clk}}\rightarrow\text{out,H}\rightarrow\text{L})</td>
<td>275</td>
<td>334</td>
<td>334</td>
<td>ps</td>
</tr>
<tr>
<td>Power (500MHz)</td>
<td>-</td>
<td>-</td>
<td>0.28</td>
<td>mW</td>
</tr>
<tr>
<td>Power (1GHz)</td>
<td>-</td>
<td>-</td>
<td>0.44</td>
<td>mW</td>
</tr>
<tr>
<td>(T_{\text{rise}})</td>
<td>169</td>
<td>178</td>
<td>-</td>
<td>ps</td>
</tr>
<tr>
<td>(T_{\text{fall}})</td>
<td>167</td>
<td>180</td>
<td>-</td>
<td>ps</td>
</tr>
</tbody>
</table>

6 Layout Design and Simulations

The 4-bit carry-select adder is implemented using CMOS 0.18\(\mu\) technology. Figure on the next page shows the layout of 4-bit adder. The rectangular dimensions of the layout are 50.80\(\mu\times 39.29\mu\), with total area of 1995\(\mu^2\). Complete listing of 4-bit adder is attached with the document. The layouts included are:

1. 4-bit Carry Select Adder.
2. 4-bit Carry Select Adder Dimensions.
3. 1-bit Stage-1 full adder (with carry in).
4. 1-bit Stage-1 full adder (with carry in = '0').
5. 1-bit Stage-1 full adder (with carry in = '1').
6. 1-bit Stage-2 full adder.
7. 2-bit Full Adder.
8. 2-bit Carry 0 adder.
9. 2-bit Carry 1 adder.
10. 2 to 1 Mux.
11. 1-bit Simplifies TSPC positive ET flip-flop

Figure attached with the layout diagram shows the waveform diagram for functional verification. Please note that 4-bit input 'B' remains constant in all the waveforms. Hence is not shown in waveform diagrams.

1. Waveform 1: B = "0000".
2. Waveform 2: B = "1111".
3. Waveform 3: B = "1010".
4. Waveform 4: B = A.

7 Characterization

The layout design is simulated for input setup time, output delays, frequency of operations and power. Table ?? summarize the input-output switching characteristics of the 4-bit adder at default 500 MHz of operations.

<table>
<thead>
<tr>
<th>Switching Parameter</th>
<th>$H \rightarrow L$</th>
<th>$L \rightarrow H$</th>
<th>Typical</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{\text{setup}}$</td>
<td>78</td>
<td>20</td>
<td>78</td>
<td>ps</td>
</tr>
<tr>
<td>$T_{\text{hold}, H \rightarrow L}$</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ps</td>
</tr>
<tr>
<td>$TC_{\rightarrow Q, \min}$</td>
<td>180</td>
<td>117</td>
<td>117</td>
<td>ps</td>
</tr>
<tr>
<td>$TC_{\rightarrow Q, \max}$</td>
<td>390</td>
<td>353</td>
<td>390</td>
<td>ps</td>
</tr>
<tr>
<td>Avg Power (500 MHz)</td>
<td>-</td>
<td>-</td>
<td>0.297</td>
<td>m W</td>
</tr>
<tr>
<td>Avg Power (1 GHz)</td>
<td>-</td>
<td>-</td>
<td>0.456</td>
<td>m W</td>
</tr>
<tr>
<td>Avg Power (1.43 GHz)</td>
<td>-</td>
<td>-</td>
<td>0.590</td>
<td>m W</td>
</tr>
<tr>
<td>Avg Power (2 GHz)</td>
<td>-</td>
<td>-</td>
<td>0.923</td>
<td>m W</td>
</tr>
</tbody>
</table>

Simulations has been done till 2GHz of operation and found to be working. Waveforms are attached for 1.43GHz and 2GHz of operations. Quality of output waveforms is not so good for 2GHz of operations.
8 Applications

As discussed in the introduction, pipelined presented in this report can be used for either generating larger (n-bit) adders or certain user specific logic can be tagged and included in the second-stage pipeline. This is because of low clock-to output delays of the MUX used. But power utilization of the adder is very high, may not be used for embedded system applications. Because of the specific nature of the adder, following applications are identified:

1. Implementation of DSP algorithms: DSP algorithms includes lot of pipeline stages, so the 4-bit pipelined adder can be used to built multi-stage n-bit pipelined adder. Only few modifications are required for this change.

2. Vector Processing

3. As a computation logic in VLSI, like computation of branch or jump target addresses, or PC next logic.

9 Conclusions

9.1 Improvements possible

Carry-select architecture is used for the implementation of the 4-bit adder. But pipelining method used in this project does not delivers the best performance for carry-select architecture.

Figure 8 shows the improved pipelined architecture, that can give better performance than what has been used for this project. This architecture has three-stage pipeline implementation. But since the single stage pipeline suffers just 1-bit full adder delay, would give better performance in terms of clock cycle or frequency of operations.

9.2 Discussion

From the detail analysis of the waveforms, there can be some interesting facts that can be pointed out.
Figure 8: Block Diagram of improved 4-bit pipelined carry-select adder.

1. All the observations done for the output of 1-bit Flip-Flop are still valid for output S0 and S1 of the adder. Since these outputs are just the outputs of the flip-flop.

2. Outputs 'S2', 'S3' and 'Cout' also suffer MUX delays together with clock to Q delay of the flop. So the clock to output delay of these signals is approximately double of what has been observed for Flip-Flop in the last lab or 2 to 1 MUX. These delays can be observed from the waveforms attached.

3. Power utilization, as can be observed from characterization table, doubles 0.297mW to 0.923mW with increase in frequency from 500MHz to 2GHz.