Performance and Area Tradeoffs in Space-Qualified FPGA-Based Time-of-Flight Systems

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Abstract - This paper introduces four FPGA-based designs for radiation-tolerant time-of-flight (TOF) systems for sub-atomic particles: Snapshot, Vernier, Fast-Clocking and Hybrid designs. The designs measure TOFs ranging from 0 to 240 ns and are compared based on resolution, thermal performance, FPGA I/O pin usage and area, particle processing rate, and power consumption. All designs are implemented and tested on an Actel ProASIC 3E A3PE1500 FPGA using only the features available on the radiation-tolerant Actel RTAX 2000 S/SL. The designs achieve resolutions of 130 ps to 25 ns and particle rates of 1.63 to 40 MHz, use from 0.02% to 7.59% of the FPGA area, and consume from 396 to 448 mW. The TOF measurements of the Fast-Clocking Design show no thermal variation across the ranges of -25°C to 55°C. The other three designs vary linearly with temperature, but this variation can be calibrated using a temperature sensor. All four designs offer a flexible, inexpensive TOF measurement system that can be implemented across a broad range of FPGAs.

I. INTRODUCTION

Time-of-flight (TOF) measurements of sub-atomic particles are central to characterizing plasma composition in space. The TOF is defined as the time it takes a particle to travel between two detection locations. Depending on the type of particle and the length of the TOF path, this time can range from several picoseconds to several microseconds. Thus timers measuring TOFs must be able to measure a large range and have a fine resolution. Many TOF measurement systems are built using Application Specific Integrated Circuits (ASICs). These ASICs achieve TOF resolutions on the order of nanoseconds using phase-locked loops (PLLs) or delay-locked loops (DLLs) to accurately boost a coarse system clock frequency, such as 40 MHz, to 1 GHz or higher.

However, ASICs are often unsatisfactory solutions for TOF systems used in space because of the low volume needed for only a small number of missions. In addition, ASICs must be radiation-hardened to be space-qualified. The manufacturing cost of producing a small number of radiation-hardened chips can cost over a million dollars per unit.

In this paper, radiation-hardened FPGAs are explored as alternatives to ASICs. In addition to the low cost and ready availability of radiation-hardened FPGAs, this solution offers flexibility of design. All four designs introduced in this paper are designed to use the Actel RTAX2000 S/SL FPGA, a space-qualified FPGA. Due to the triple redundancy in the RTAX logic, many high-end FPGA features are absent, such as clock managers and PLLs. Despite these limitations, all four FPGA-based TOF designs introduced in this paper are successfully implemented using only this limited functionality.

II. TOF DESIGNS

This section describes each of the four TOF designs and their methods of TOF calculation. All designs assume start and stop pulses of 70 ns width that indicate the entrance and exit, respectively, of a particle through a pair of detectors such as Channel Electron Multipliers (CEMs). The designs are implemented on an Actel ProASIC 3E FPGA because its reprogrammability makes it ideal for testing. However, the designs use only features available on the comparable radiation-tolerant, anti-fuse-based RTAX2000.

A. Snapshot Design

The Snapshot Design uses only flip-flops and buffers, as shown in Figure 1. The start pulse is sent down a delay line composed of buffers, which have delays specific to a given FPGA. Each buffer output is also connected to the data input of a flip-flop. The stop pulse is connected to the clock input of each flip-flop. Thus, when the stop pulse arrives, the flip-flops take a snapshot of the location of the start pulse along the delay line.

Figure 1. Snapshot Design block diagram

The TOF is determined using Equation 1, where \( t_b \) is the delay of a single buffer and \( N \) is the number of buffers the start pulse has traversed.

\[ \text{TOF} = t_b \times N \quad \text{Eq. 1} \]
B. Vernier Design

The Vernier Design uses two ring oscillators of different frequencies. A primary oscillator begins oscillating when the start pulse arrives, and a secondary oscillator begins oscillating when the stop pulse arrives. Eventually the primary and secondary oscillators reach coincidence. A block diagram of the Vernier Design is shown in Figure 2.

![Figure 2. Vernier Design block diagram](image)

The TOF is determined by the number of oscillations made by each oscillator before coincidence, as given in Equation 2. \( T_p \) and \( T_s \) are the clock periods of the primary and secondary oscillators, respectively, and \( N_p \) and \( N_s \) are the number of oscillations of each oscillator before coincidence is reached.

\[
TOF = T_p \times N_p - T_s \times N_s \quad \text{Eq. 2}
\]

An example is shown in Figure 3. Oscillator 1 has a period of 5 ns and oscillator 2 has a period of 4 ns. Oscillators 1 and 2 oscillate four and two oscillations, respectively, before they reach coincidence. Thus the measured TOF is 12 ns.

![Figure 3. Vernier Design sample timing diagram](image)

C. Fast-Clocking Design

The Fast-Clocking Design counts the number of rising system clock edges between the start and stop pulses to determine the TOF. A block diagram of this design is shown in Figure 4.

![Figure 4. Fast-Clocking Design block diagram](image)

The resolution of the design is the system clock period, \( T_c \). The TOF is calculated using Equation 3, where \( N \) is the number of clock cycles between the start and stop pulses.

\[
TOF = T_c \times N \quad \text{Eq. 3}
\]

D. Hybrid Design

The Hybrid Design combines the Snapshot and Fast-Clocking Designs. The Fast-Clocking Design makes a coarse TOF measurement. Then two modified Snapshot Designs are used to make a finer measurement. The modified Snapshot Designs measure the delay between the rising edge of the start or stop pulse and the preceding system clock rising edge. A block diagram of this design is shown in Figure 5.

![Figure 5. Hybrid Design block diagram](image)

In the modified Snapshot Designs, the system clock travels down the delay line and either the start or stop pulse, depending on the modified Snapshot Design, is sent to the clock input of the flip-flops. Figure 6 shows the regions measured by the system clock and the regions measured by the modified Snapshot Designs.

![Figure 6. Hybrid Design timing diagram](image)
The TOF is calculated using Equation 4, where $T_c$ is the system clock period, $N$ is the number of clock cycles between the start and stop pulses, and $T_1$ and $T_2$ are the measurements made by the start and stop Snapshot Designs, respectively. $T_1$ measures the delay between the system clock rising edge and the start pulse rising edge, and $T_2$ measures the delay between the system clock rising edge and the stop pulse rising edge, as shown in Figure 6.

$$TOF = T_c \times N - T_1 + T_2 \quad \text{Eq. 4}$$

Jin proposes an alternative hybrid design combining Fast-Clocking and Vernier methods [5]. Aloisio combines a Fast-Clocking method with delay lines created from carry chains on the FPGA [6].

### III. DESIGN PERFORMANCE AND COMPARISON

The four designs are evaluated and compared based on maximum resolution, measurement accuracy, thermal performance, FPGA I/O pin usage and area, particle processing rate, and power consumption. The experimental results are shown in Table 1. The highlighted boxes indicate the design that performs the best in each category.

<table>
<thead>
<tr>
<th></th>
<th>Snapshot Design</th>
<th>Fast-Clocking Design</th>
<th>Hybrid Design</th>
<th>Vernier Design</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Maximum Resolution</strong></td>
<td>130 ps</td>
<td>Clk freq.</td>
<td>130 ps</td>
<td>2.3 ns</td>
</tr>
<tr>
<td><strong>Thermal Variation</strong></td>
<td>Linear</td>
<td>None</td>
<td>Linear</td>
<td>Linear with Oscillator</td>
</tr>
<tr>
<td><strong>FPGA Output Pins</strong></td>
<td>9</td>
<td>4 with 40 MHz Clk</td>
<td>16</td>
<td>12</td>
</tr>
<tr>
<td><strong>Logic Blocks</strong></td>
<td>2,867 (7.5%)</td>
<td>7 (0.02%)</td>
<td>2,138 (5.6%)</td>
<td>134 (0.4%)</td>
</tr>
<tr>
<td><strong>Particle Rate</strong></td>
<td>3.2 MHz</td>
<td>4.1 – 40 MHz</td>
<td>4.1 – 14.3 MHz</td>
<td>1.63 – 14.3 MHz</td>
</tr>
<tr>
<td><strong>Power</strong></td>
<td>432 mW</td>
<td>414 mW</td>
<td>448 mW</td>
<td>396 mW</td>
</tr>
</tbody>
</table>

*Table 1. Design Performance and Comparison*

#### A. Maximum Resolution

The maximum resolution is defined as the smallest TOF that the system can accurately identify. The resolutions of all designs are tested using a Stanford Research Systems DG645 delay generator, which has a resolution of 5 ps.

The Snapshot Design has the highest maximum resolution of the four designs. The delay through a logic block on the ProASIC 3E FPGA is 540 ps, which was confirmed through testing. The resolution of the Snapshot Design can be pushed to 130 ps by eliminating the buffers from the delay line and using only the routing delay in the FPGA.

The resolution of the Vernier Design is limited by the difference in periods between the two ring oscillators, which have 30.9 ns and 28.6 ns clock periods in the tested system. The achieved resolution is worse than the Snapshot and the Hybrid Designs at 2.3 ns.

The Hybrid Design has the same resolution as the Snapshot Design of 540 ps. The resolution of the Hybrid Design can again be increased to 130 ps by eliminating the buffers along the delay lines and using the routing delay in the FPGA.

The Fast-Clocking Design has the worst resolution of the four designs at 25 ns, the period of the FPGA system clock. A faster system clock would increase this design’s resolution, but typical space-qualified FPGAs can only run as fast as 500 MHz, limiting the resolution to 2 ns.

Unlike the Snapshot and Vernier Designs, the Fast-Clocking and Hybrid Designs are synchronous systems. Because start and stop enter these systems asynchronously, metastability can occur when either pulse enters these systems during the aperture time of a flip-flop. Depending on when the pulses enter the system, synchronizers may be necessary.

#### B. TOF Measurement Accuracy

All four designs successfully compute TOFs ranging from 0 to 240 ns. The designs are tested in 5 ns increments from 0 to 240 ns with 5 ps accuracy using the Stanford Research Systems DG645 delay generator. The measured TOFs for the Snapshot Design are shown in Figure 7, with a slope of 0.9805 and an R-squared value of 0.9994.

![Snapshot Design measured TOFs](image)

The measured TOFs for the Vernier and Hybrid Designs show the same linear behavior as the measured TOFs for the Snapshot Design with slopes of 1.0015 and 0.9995, respectively, and an R-squared value of 0.9999 for both designs.

The measured TOFs for the Fast-Clocking Design are shown in Figure 8, with a slope of 0.9977 and an R-squared value of 0.9951. At certain TOFs the Fast-Clocking Design
measured TOF oscillated between two values, which are averaged to create a single TOF measurement.

**Figure 8. Fast-Clocking Design measured TOFs**

C. Thermal Performance

The TOF systems must be able to withstand thermal variations in space. The four designs are tested at a TOF of 100 ns from -25°C to 55°C using a Thermotron SE Environmental Test Chamber. This is the military operating temperature range of the ProASIC 3E and RTAX2000 S/SL FPGAs. The Snapshot, Vernier, and Hybrid Designs vary with temperature. However, each system can be calibrated using a fixed ring oscillator to measure and adjust for temperature change.

The Snapshot Design varies linearly with temperature with a slope of -0.114 ns/°C, as shown in Figure 9. As temperature increases, the delay through a logic cell increases, causing the measured delay to decrease.

**Figure 9. Snapshot Design thermal performance**

For the same reason, the periods of the ring oscillators in the Vernier Design increase as temperature increase, as shown in Figure 10. The slope of the period of the first oscillator is 0.035 ns/°C. The slope of the period of the second oscillator is 0.033 ns/°C. The varying periods of the ring oscillators cause the measured TOF to vary with temperature as shown in Figure 11. The saw-tooth pattern emerges due to the bin size of the Vernier Design and the linear change of each oscillator. Each “tooth” is generated from the delay falling into a particular bin, and the linear relationship within each bin comes from the linear change in the periods of the oscillators.

**Figure 10. Vernier Design thermal performance of oscillators**

The Fast-Clocking Design, which depends on a crystal oscillator and not logic cells, shows no change with temperature, as shown in Figure 12.

**Figure 11. Vernier Design thermal performance**

**Figure 12. Fast-Clocking Design thermal performance**
The Hybrid Design shows linear temperature variation in the Snapshot portions of the design. However, the design shows no thermal variation when tested at a TOF of 100 ns, as shown in Figure 13, because the test TOF is a multiple of the system clock period. In this case, the clock travels through the same number of buffers in both modified Snapshot Designs. Since the TOF is calculated by taking the difference between the two Snapshot delays, the temperature variation is canceled. However, for TOFs that are not multiples of the clock period, the clock travels through an unequal number of buffers in the modified Snapshot portions of the design and the temperature variation in the two delay lines does not cancel.

The Fast-Clocking Design uses the least FPGA area at less than 0.02% of the ProASIC 3E FPGA. The Fast-Clocking Design requires only a system clock and a counter. The Vernier Design, consisting of two ring oscillators, two counters, and a coincidence detector, uses slightly more FPGA area at 0.4%.

The Snapshot and Hybrid Designs require significantly more hardware due to the number of flip-flops and buffers in the Snapshot Design. The delay lines also require extra hardware to encode the flip-flop outputs into binary representations of the TOF measurements. The Hybrid Design occupies 5.6% of the FPGA area, which includes 92 buffers and 92 flip-flops for two 25 ns delay lines at a 540 ps resolution. The area required for the delay lines can be reduced if the system clock frequency is increased. The Snapshot Design occupies the most FPGA area at 7.5% because it includes 437 buffers and 437 flip-flops. For larger ranges of TOF measurements, the Snapshot Design area increases proportional to the increase in range while the Hybrid Design area stays relatively constant.

E. Particle Rate

The particle rate is the number of particles that the system can process per second. The Snapshot Design requires 310 ns for each start pulse to completely traverse the delay line, regardless of the actual TOF: 240 ns for the length of the delay line plus 70 ns for the width of the pulse. Thus, the particle rate is 3.2 MHz across all TOFs. The Fast-Clocking Design counts the number of system clock cycles between the rising edges of the start and stop pulses, so its particle rate is limited only by the TOF of the particle and the 25 ns resolution. The particle rate is 4.1 to 40 MHz to measure TOFs ranging from 0 to 240 ns. The lower limit on the particle rate is determined by the maximum TOF the system can measure.

The Hybrid Design particle rate is also limited only by the TOF of the particle and the resolution of the Fast-Clocking portion of the design. Recall that the Snapshot portions of this design have clock running through the delay lines, so the width of the start and stop pulses do not limit the particle rate. Thus, the Hybrid Design can also achieve particle rates of 4.1 to 40 MHz, depending on the particle TOF.

The Vernier Design must wait for its ring oscillators to come into phase before it can determine the TOF and take the next TOF measurement. The period of the secondary oscillator can be defined as $T_p = D$, where $T_p$ is the period of the primary oscillator and $D$ is the difference in the periods of the two ring oscillators. $N_p$ and $N_S$ are the number of oscillations of the primary and secondary oscillator respectively before the oscillators reach coincidence. The measured TOF is then given by Equation 5.

$$\text{TOF} = T_p \times N_p - N_S \times (T_p - D) \quad \text{Eq. 5}$$

Since the secondary oscillator is used to measure a time less than the period of the primary oscillator, each oscillator is guaranteed to oscillate an equal number of times prior to coincidence. $N_S$ can be related to $N_p$ by the number of whole,
unmatched, primary oscillations before the stop signal is observed. This is given by Equation 6.

\[ N_S = N_P - \frac{TOF}{T_P} \]  

Eq. 6

By combining Equations 5 and 6, \( N_P \) can be related to the TOF of the system by Equation 7. Since fractional oscillations cannot be observed, the ceiling is taken.

\[ N_P = \left( \frac{TOF}{T_P} - \frac{TOF}{D} \right) \left( \frac{T_P}{L} - e \right) \]  

Eq. 7

This equation produces a maximum of 20 oscillations before coincidence is reached at a TOF of 214 ns, which gives this design a worst-case particle rate of 1.63 MHz. In the best case the oscillators reach coincidence before the falling edge of the 70 ns stop pulse. The next set of start and stop pulses can be processed immediately after that falling edge. For a TOF of 0 ns, the minimum time between sets of start and stop pulses is limited by the pulse width of 70 ns, giving the Vernier Design a maximum particle rate of 14.3 MHz.

F. Power Consumption

The current and voltage of the FPGA development board are monitored during TOF calculations to record the maximum power consumption for each device. These power values do not directly transfer from the flash-based ProASIC 3E FPGA to the anti-fuse-based RTAX 2000 S/SL because the static power and start up power are architecture specific. However, the relative power consumption between designs stays the same across architectures because dynamic power is proportional to the number of gates for a given design. The Vernier Design uses the least amount of power, 396 mW, because the gates do not switch when no signals are observed and it only uses a small number of gates.

V. CONCLUSION

Four TOF measurement systems were designed, built and tested: the Snapshot, Vernier, Fast-Clocking, and Hybrid designs. Each design successfully computes the TOF from 0 to 240 ns and can be implemented on space-qualified FPGAs, such as the Actel RTAX2000 S/SL, using only combinational logic, flip-flops, and counters.

Snapshot and Hybrid Designs both achieve the highest resolution of 130 ps. The Snapshot Design requires the most FPGA area, 7.5%, while the Hybrid Design uses only 5.6%. This disparity increases with larger TOF ranges. The Fast-Clocking Design uses only 0.02% of the FPGA and achieves a particle rate of 4.1 to 40 MHz. However, its resolution is the worst of the four designs at 25 ns, or the system clock period. A higher frequency system clock will give a higher resolution. The Vernier Design has a higher resolution than the Fast-Clocking Design at 2.3 ns while still maintaining a small FPGA area, using only 0.4% of the FPGA. The Vernier Design also achieves a slightly lower operating power, 396 mW, than the other designs. The Fast-Clocking Design is the only design that exhibits no variation across temperatures. The linear temperature variations in the Snapshot, Vernier, and Hybrid Designs can be corrected using an additional fixed ring oscillator to measure temperature change.

Several optimizations include the following. The FPGA area of the Snapshot Design can be reduced by increasing the delay between each flip-flop in a pseudo-logarithmic manner. The resolution of the Vernier Design can be increased by decreasing the difference between oscillator periods, but this comes at a cost of a decreased particle rate. The Fast-Clocking and Hybrid Designs can be improved by including hardware to account for metastability, and the FPGA area required by the Hybrid Design can be reduced if the system clock has a frequency higher than 40 MHz.

Future steps include evaluating these improvements and optimizing performance for the next generation of spaceflight instrumentation.

VI. ACKNOWLEDGEMENTS

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REFERENCES
