

Design & Analysis of 6-bit Dynamic Manchester Carry Chain

Adder in 0.18 CMOS process

I. Abstract

This project is to implement the 6-bit Manchester Carry Chain Adder in 0.18um CMOS process with 4 metal layers for an ALU to be used in a high performance or mobile microprocessors.

We start with analyzing the design criteria followed by choosing the adder architecture and the logic style for every logic block considering the trade-off among every criterion. After this, we make the schematic design & simulation, estimating for some parameters and performance for this design. At last, we work on the layout design & simulation, getting the more accurate data for analysis with the extracted parasitic model.

In addition to these steps, special optimizations (such as transistor sizing and adding buffer) are employed in this design to meet the stated design constraints such as propagation delay and the utilization of system resources (area and power consumption).

II. Background

The adders being one of the most necessary modules in any performing design numerical computations, a lot of research work was done in determining an ideal design that works at the lowest possible delay, least area and also consuming the lowest amount of power possible. Based on the prevailing technologies, it was not possible to design an architecture that satisfies all the above criteria. While designing an adder, above three characteristics (area, delay and power) have to be sacrificed in order to result in an optimal design that accepts values of the other one or two.

The implementation for this design is based on 0.18um CMOS process, and our design has been through several steps shown as follows:

- A. Implement transistor level schematic with Cadence-composer.
- B. Verify schematics design for functionality and test for performance using Cadence's SpectreS.
- C. Perform layouts of the above designs using Cadence's Virtuoso.

- D. Check the layout with DRC & LVS.
- E. Perform parasitic extraction on the layout with RCX.
- F. Extract Pin-only model for simulation.
- G. Verify schematics design for functionality and test for performance on extracted layout design.
- H. Compare the results obtained from extracted layout with the results from the schematics and analyze the reason.

III. Design Criteria

There are many criteria in this design, all of which contribute to making a decision of choosing the adder architecture and logic style. In addition, some requirements are not explicit, so we need to analyze and convert it to obvious criteria, which can be easily tested in the simulation. The design criteria and constraints are listed in the following table with analysis.

Criteria	Specification & Analysis
Technology	0.18um CMOS
Power Supply	for simplicity, use 1.8V
Area	Not specified, as small as possible
*Worst Case Delay	Not exceed 10 fanout-of-4 (see analysis below)
Rise & Fall Time	Not exceed 200ps
Noise Margin	At least 10%
*Load Capacitance	2mm*1um Metal5 in layout (see analysis below)
Input Capacitance	No more than 50fF in previous stage
Power-Delay-Product	Not specified, as small as possible

Note that the constraints of worst case delay and load capacitance is not explicit, but we can either calculate with formula or simulate with layout to estimate these two criteria, which is shown as follows:

For worst case delay, we can calculate with the formula about the inverter chain:

$$T_p = N \times T_{p0} (1 + f / \gamma)$$

In this design requirement, N=10, f=4 (fan-out factor of approximately 4 per stage leads to minimal delay) and Tp0=25ps. We suppose $\gamma=1$, so we can estimate the worst case delay criteria is not exceed 1250ps.

For load capacitance, the requirement is that the adder is driving a 2mm*1um (M5) bus with two loads evenly distribute in along the bus. Each capacitive load is equal to the adder input capacitance. The total capacitance is bus capacitance and the adder input capacitance. We draw a 2mm*1um (M5) bus in layout and extract it with RCX and get the result of 116.8fF for the bus. For input capacitance, we can also estimate

the result of $2 \times 12\text{fF}$. So the total load capacitance is approximately 141fF .

IV. Design Analysis

In this project, much architecture can be employed to implement this 6-bit adder. But considering the all factors (delay, area and power consumption), two way of design stand out others.

One way is using Logarithmic architecture, whose main advantage is the quickness of getting the computation result of carry bit, which is very important in reduce the propagation delay when designing multilevel adder (such as 64-bit or much bigger). For a 64-bit adder, the propagation delay of a logarithmic adder is proportional to 6, compared to 64 for a linear adder. However, it brings some structural complexity to the design as a trade-off.

Another attractive structure is Manchester Carry Chain, which uses a cascade of pass transistors to implement the carry chain. The main advantage of Manchester Carry Chain is it is simpler in structure and can be easily modularized in the schematic and layout design. In addition, the performance of quickness is also good, especially using dynamic implementation.

Comparing these two architectures, I prefer Manchester Carry Chain because of the structure and amount of transistors, which can make the schematic and layout design simpler. And another reason is the advantage of Logarithmic architecture is less obvious in designing a 6-bit adder. So it is not worth the cost of circuit complexity any more.

For Manchester Carry Chain architecture, another decision should be made that whether use the static or the dynamic implementation. The advantage of static implementation is the robustness of the output signal, the less power consumption and the maximum noise margin. But it is at the cost of the performance in propagation delay, because in every signal transition, there must be a charge or discharge from VDD to output or from output to GND. In ALU design, the propagation delay is most important, so we turn the focus into the dynamic ones.

The amount of transistors in dynamic implementation is same as in static ones, so it does not bring any complexity in design. And the clock load is not heavy in this design (only $12+2$ clock loads), which is a trivial cost compared with improvement it brings in performance. However, the transistors must be carefully sized to prevent race problem and clock chew.

Based on the analysis above, we decide to choose dynamic Manchester Carry Chain architecture to implement 6-bit adder.

V. Solution

The implementation of Manchester Carry Chain Adder is based on the Propagate & Generate model. The Propagate path passes C_{in} to the C_{out} if the propagate signal ($A_i \oplus B_i$) is true. And the Generate unit ensures that a carry bit will be generated at C_{out} independent of C_{in} if the generate signal ($A \& B$) is true.

Figure 1 shows a dynamic version of 1-bit Manchester Carry gate. Since the transitions in a dynamic circuit are monotonic, the transmission gates can be replaced by NMOS-only pass transistors, and precharging the output eliminates the need of kill signal in static version.

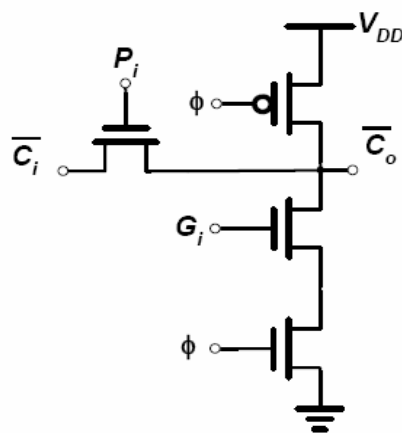


Figure1 1-bit Manchester Carry Gate

The basic idea of the Manchester Carry Chain is using a cascade of pass transistors to implement the carry chain. An example of a 5-bit dynamic Manchester Carry Chain adder is shown as follows:

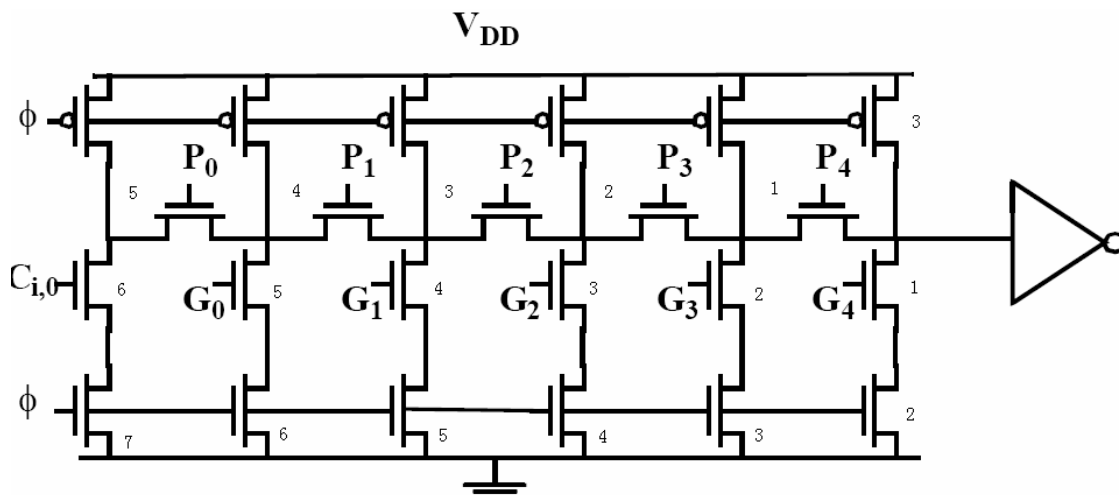


Figure2 5-bit dynamic Manchester Carry Chain Adder (carry section)

We can see from the figure 2 that during the precharge phase (CLK=0), all intermediate nodes of the pass transistor carry chain are precharged to VDD. During the evaluation, the nodes is discharged when there is an incoming carry and propagate signal Pk is high, or when the generation signal Gk for stage k is high.

Another important issue for this design is the transistor sizing. The complete sizing for the 5-bit Manchester Carry Chain adder example is shown above: the number represents how many times the width of transistor compared to the minimal size in the figure (In 0.18um technology, we assume the minimum size is W = 0.22um and L = 0.18um).

The sizing is based on the following formula to get the minimal worst case delay of the carry chain of the adder.

$$T_p = 0.69 \sum_{i=1}^N C_i \left(\sum_{j=1}^i R_j \right)$$

So we applied this sizing principle to our schematic design, which is shown in the subsequent section.

VI. Schematic Design & Simulation

After analyzing the solution of this design, we will perform the schematic design in the following important elements.

A. Generate Unit

The schematic of Generate Unit is shown in Figure 3. In this design, we use static complementary CMOS to implement it instead of dynamic style because it avoids the problems caused by using the different clock and reduce the clock loads. And another advantage is that it guarantees a robust input to the Manchester Carry Chain.

Figure 4 shows the functional verification and design characteristics of Generate Unit, and parameters collected and calculated from Figure 4 are depicted in the table.

Worst Case Delay	93 ps
Iaverage	1.57E-6 A
Power-Delay-Product	2.628E-16 J

B. Propagate Unit

The schematic of Propagate Unit is shown in Figure 5. In this design, we use static implementation for the same reason, and the transmission gate implementation decrease the amount of transistors to 6 and keep a good performance.

Figure 6 shows the functional verification and design characteristics of Propagate Unit, and parameters collected and calculated from Figure 6 are depicted in the table.

Worst Case Delay	50 ps
Iaverage	8.422E-7 A
Power-Delay-Product	7.58E-17 J

C. Inverter Chain Buffer

In this design, since the adder will drive load capacitance in the output, so we need this inverter chain buffer to improve the performance of the MCC adder. The schematic of Inverter Chain Buffer is shown in Figure 7.

D. MCC Adder Bit 0 to Bit 5 Unit

The schematic of these 6 units are shown in Figure 8 to Figure 14. We can see from the schematic that every output is added an inverter chain buffer, and the main difference among these units is the transistor size.

Figure 9 shows the functional verification and design characteristics of MCC Adder Bit0 Unit, and parameters collected and calculated from Figure 9 are depicted in the table.

Worst Case Delay	37 ps
Iaverage	2.841E-5 A
Power-Delay-Product	1.89E-15 J

E. Complete 6-bit MCC Adder

After designing 6 bit units respectively, we can assemble them together to implement the complete schematic, which is shown in Figure 15. In this figure, the critical path is highlighted with yellow pen. (we assume C0 is always 0 and the sum module is slower than the MCC)

A test circuit for this adder is shown in Figure 16. From the figure we can see every output drives a capacitance of 141fF which is calculated in Criteria section. For worst case delay simulation, we consider A=111111, B=000001 and C=0 as the signal input. Simulation and test graph are shown in Figure 17 to Figure 19.

Figure 17 shows the worst case delay test using the above input. Notice that the waveform of S0 is different from other output. It is mainly because the C0 input signal in Figure 9 is directly connected to the second XOR gate to generate S0 output. So S0 is not affected by the clock. To change the waveform of S0 to the same form as

other outputs, we only need to add an inverter connected between the M node (in Figure 8) and the second XOR gate.

The parameters collected and calculated from Figure 17 and Figure 19 is depicted in the table.

Worst Case Delay	587 ps
Iaverage	1.247E-3 A
Power-Delay-Product	1.318E-12 J

In Figure 18 and Figure 19, a noise margin test and a rise & fall time test are performed respectively. It turns out to meet the corresponding design criterion.

VII. Layout Design & Simulation

Based on the schematic, we develop the layout design for every basic cell described in schematic design and check them with Assura DRC and LVS to guarantee that the layout meets the design rule and the layout design matches the schematic design. The layout is shown in Figure 20, 22, 24, 26, 28, 30, 32, 34, 36, 38 and 40 respectively. Figure 41 shown the DRC & LVS check result for the complete 6-bit MCC Adder layout.

After rough measuring with the ruler in Cadence, the area of the final design is $19.900 \times 106.200 = 2113.38$ square microns (The exact area is shown in Figure 40(2)).

After this step, we perform RC extraction using Assura RCX for every basic cell, and the extraction model for every basic cell is shown in Figure 21, 23, 25, 27, 29, 31, 33, 35, 37, 39 and 42 respectively.

From now on, we can use the extraction model in Figure 42 to generate the parasitic model for the simulation work. The same simulation as the schematic is performed to compare the results generated both by schematic and parasitic model.

The transient response for the similar simulation tests is shown in Figure 43 to Figure 45. Figure 43 shows the worst case delay test using the previous input as in Figure 17. The parameters collected and calculated from Figure 43 are depicted in the table.

Worst Case Delay	610 ps
Iaverage	1.251E-3 A
Power-Delay-Product	1.374E-12 J

In Figure 18 and Figure 19, a noise margin test and a rise & fall time test are performed respectively. It also turns out to meet the corresponding design criterion.

After analyzing the data collected from the simulation result, we found almost all the parameters become a bit worse for the layout design compared with the schematic one. It is mainly because that after extraction, the simulation based on layout design considers more factors and uses more precise parameter. In other words, it is more close to the real performance of the devices.

VIII. Discussion

There are two interesting phenomenon which is worth notice. The first one is that in Figure 17 we get the last carry bit C6/S6 ahead of the S5 and in layout simulation we get C6/S6 even early than S4. It may result from the special structure of the Manchester Carry Chain which takes more time in sum generation module and less time in propagating the carry bit signal. This characteristic is beneficial to the adder because the most significant bit does not need wait a long time for the carry bit signal from the previous stage. If the carry bit signal is propagated much quickly than the sum generation module, the efficiency of the adder is improved because it is possible that every bit unit will do the addition in parallel. For a larger adder, the improvement might be more obvious.

Another phenomenon is clock feedthrough. Looking at Figure 9, Clock feedthrough problems can be seen in the output signal C1_INV when low to high, and it also happens in other output such as C2_INV to C5_INV. But fortunately, it can not result in malfunction in this design. For slower clock, it performs better than this situation. The clock feedthrough is mainly caused by the capacitive coupling between the clock input of the precharge device and the dynamic output node. The capacitive coupling causes the output of the dynamic node rise above V_{dd} on the low to high or high to low transition of the clock.

Besides, there still is a problem we need notice. That is, we size all the transistors with the reference of 220 nm as the minimum size, but actually it might not be most optimized size for the best performance. We use 220 um as reference just for convenience and the consideration of area. But chances are that the reduced area has caused worse performance as a trade-off without any notice from us. Maybe choosing a larger size will be more effective to improve the performance for this adder, but it also increases the design complexity.

IX. Conclusion

In this project, we implement a 6-bit Manchester Carry Chain adder with the implementation of dynamic circuits including complementary CMOS and TG logic. After analyzing all factors such as power consumption, delay, area and the circuit complexity, decision is made to make a trade-off among these factors to meet all the

design requirements.

From the layout simulation results, we can find out it is close to the results of schematic simulation, and the layout simulation results are only greater than the schematic results a little bit. So the schematic greatly help us estimate the simulation result. But we also need a careful layout design, which may be closer to the real situation which considering parasitics (intrinsic and routing capacitances and resistances).