Abstract:

In this project, a low-noise fully differential opamp with common mode feedback and bias network is designed for the switch-capacitor type amplifier to meet the given design specification. Calculation and approximation of some parameters are performed in advance and then simulations are run to verify the calculation. Based on the simulation and calculation, we adjust some circuit parameters (transistor size or multiplier) to meet all of the design requirements.

Circuit Selection:

First of all, we need to determine which kind of transistor do we use as input. PMOS input transistors have a higher speed because of larger V_{eff}. and it also has smaller 1/f noise. but also reduced gain and increased thermal noise. Folded cascode has priority over current mirror and two-stage amplifier, because more current goes through input transistor pair thus increasing g_m which help to reduce thermal noise.

In addition, wide-swing constant-transconductance bias circuit is employed because the design has a tight constrains about output swing. Constant transconductance biasing topology is chosen to make opamp stability and DC point independent of process variation.

CMFB is chosen to be continuous type since this kind of feedback circuit have a simpler structure and will introduce common mode signal.

Analysis:

Figure 1-3 shows the bias network, CMFB and folded cascode amplifier with transistor size respectively and Figure 4 shows the entire fully differential OTA.

For biasing circuit comes from Martin's textbook and the similar transistor size are applied to this design and circuit is redesigned for 0.35um technology.

Folded cascode Amplifier is designed so that bias current at the output stage is equal to the bias current in the input transistors. PMOS cascode transistors are design equally with 200mV overdrive voltage. Big transistors are chosen to provide more current (higher gain and slew rate) and reduce 1/f noise. In this design, hand analysis didn't help muxh, because transistor should be design precisely in order to keep all transistors in output stage in saturation. Final sizes are completely determined by simulation.

Simulation:

Test circuit for the fully differential OTA is shown in Figure 7. Gain and phase figures are plotted in the Figure 6. Phase margin of 82.29 degrees from Figure 7 guaranties system stability. From the graph and the calculation it is clear that there is no slew rate limitation.

After testing the OTA, we test entire switch-capacitor amplifier implemented by this fully differential OTA. Figure 5 shows the test circuit and the clock P1 and P2 is designed to get a 200Khz sampling frequency. Transient behavior is shown in the Figure 9, which output voltage swing is from 0.408V to 2.884V with the C_A=1.4pF, which basically meet the requirement of this design.

In addition, noise analysis is done with the simulation, Thermal noise is less than maximum value required (Figure 8). Power dissipation is 4.102mW and it is below power budget of 5mW.

Summary:

A low-noise fully differential opamp is design for switched-capacitor amplifier. Almost all design specifications are met: power dissipation, output voltage swing, slew rate limitation. System noise is much less than the design requirement, which makes this opamp in general suitable for low noise, switched-capacitor application.

However, the design is far from finished version due to the limit time. OTA transistors should be resized to smaller area. Although reducing area may result in increased noise and reduced output swing, it is worth to do it because the system noise is much less than the design specification. Further efforts would be make to get a more balanced trade off between noise, output swing, power dissipation and the area.