

Shielding Methodologies for VLSI Interconnect

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Abstract—As the technology advances into deep sub-micron era, crosstalk reduction in VLSI interconnect has become more important for high speed digital circuit design. Shielding is an effective and common technique to deal with signal integrity issues such as crosstalk noise and delay uncertainty. In this survey paper, the basic idea of shielding to reduce capacitive and inductive coupling effect is presented respectively. The effectiveness of shielding is discussed based on simulation results in different shielding cases. Shield insertion algorithms are introduced to minimize the routing area under the given noise specifications. Conclusions are drawn and discussions are made regarding the existing and future work.

I. INTRODUCTION

Interconnect crosstalk noise are regarded as one of the most critical problems that designer need to address for the deep sub-micron (DSM) design. Shielding is an effective and common technique to reduce crosstalk noise as well as delay uncertainty at the cost of increased routing area.

Capacitive coupling effects between two adjacent wires is a major concern in DSM design because the wire thickness is usually greater than wire width and the spacing between two wires is smaller than the distance between adjacent metal layers [1]. Capacitive coupling effect is a short range effect which only exists between two adjacent signal lines and it has two deleterious effects on signal integrity. When signal switches on the aggressor line, noise is induced on the victim line which might result in logic malfunction. And when both the aggressor line and victim line have signal switching event, a change in the timing of signal transition, called delay uncertainty, occurs in the victim lines [2]. Fig. 1 shows both the effect due to coupling capacitance.

On-chip inductance impacts have become more significant with the technology scaling and increase of clock frequencies. Some researches have found the

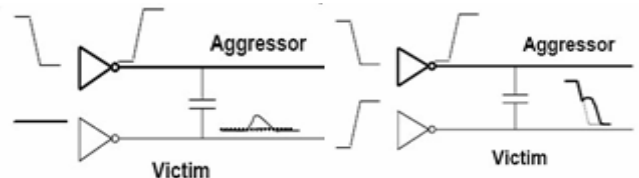


Fig. 1. Crosstalk noise and delay uncertainty due to coupling capacitance

impact of inductive coupling is comparable to capacitive effects [3]. Unlike capacitive coupling effects, inductive coupling is long range issues, so it can not be neglected between two non-adjacent signal lines. In addition, the current return path usually cannot be determined in advance in complex integrated circuits [4]. That is, without specifying current return path, the inductive coupling can not be clearly estimated. All of these characteristics add complexity for reducing this effect.

Due to capacitive and inductive coupling effects, inserting a shield line is necessary to keep the signal integrity efficiently. The rest of this paper is organized as follows: In section 2, in addition to talk about shielding strategy, we introduce another approach, spacing, to reduce interconnect coupling effect and make a comparison between these two techniques. Section 3 presents the basic idea of shielding and shows how the shield lines reduce the capacitive and inductive coupling noise respectively. In section 4, we discuss the effectiveness of shielding, and figure out which parameter and how large these parameters determine the shielding effectiveness. In section 5, Shield insertion algorithms under the condition which is close to the practical circumstance are introduced to minimize the routing area under the given noise specifications. We conclude and discuss the current and future work of shielding methodologies in the end.

II. COUPLING NOISE REDUCTION TECHNIQUES

There are two commonly used techniques to reduce

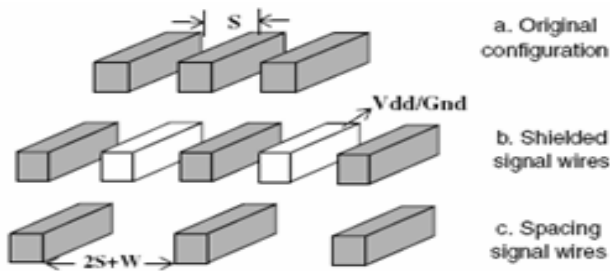


Fig. 2. Comparison of shielding and spacing strategy

coupling effects, one approach is inserting a shield line (shielding), and the alternative method is increasing the interline space (spacing) [5]. Each of them has its advantages and drawbacks. Fig. 2 illustrates these two approaches respectively.

Shielding can avoid the undesirable increase in coupling capacitance and the important benefit of shielding is that it can reduce inductive coupling noise. However, shielding consumes more power, increases routing area and add interconnect complexity.

Alternatively, wire can be simply spaced apart to produce the similar solution. Although spacing does not eliminate capacitive coupling noise, it reduces coupling noise as well as power dissipation because the total capacitance load of the lines decreases, contrary to the increase of total capacitance load for shielding strategy.

Therefore, in the cases that which inductive coupling is not evident and low power is more important, spacing is still in use. In most cases, both shielding and spacing are employed for different situations. But as technology scales, shielding will become more preferable.

III. BASIC IDEAS OF SHIELDING

The basic idea of shielding is to insert a wire directly connected to power/ground line between the two signal lines. Fig. 3 shows the shield insertion and its effect on the previous coupling capacitance and inductance.

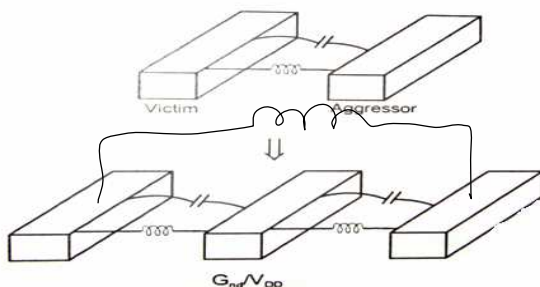


Fig. 3. Circuit model of shielding and its effects on signal lines

We can see from Fig. 3 that by inserting a shield line between the two adjacent signal lines, the coupling

capacitance between the two signal lines disappear which is replaced by two new coupling capacitance between the signal line and shield line. Therefore, shield line efficiently isolates the voltage switching activities of the neighboring lines due to coupling capacitance.

For reducing inductive coupling noise, shield line provides a closer and clearly defined current return path for both the signal lines [4], so the mutual inductive effect are reduced significantly compared to spacing strategy. However, the inductive coupling can not be eliminated by just inserting a shield lines because the mutual inductance still exists between the two signal lines (Fig. 3).

IV. EFFECTIVENESS OF SHIELDING

For further design the shielding strategy for different circuits, what factor and parameter and how large these factors and parameters have impacts on the shielding effectiveness of the victim lines need to be figured out. A lot of researches [3][4][5] focus on this topic with a simplified shielding structure model. In this section, several parameters and shielding patterns such as shield material, geometric characteristics of the shield lines and signal lines, separation between two lines and number of connection tied the shield line to the ground are investigated and discussed.

A. Materials of wires

We start with a brief comparison of crosstalk effect for copper and aluminum, which is commonly used in high speed interconnect. Fig. 4 shows this comparison under different width and space of the signal lines. Although Al lines have a larger crosstalk noise due to thicker metal layers, Cu lines exhibit an increased noise trend when the width is large.

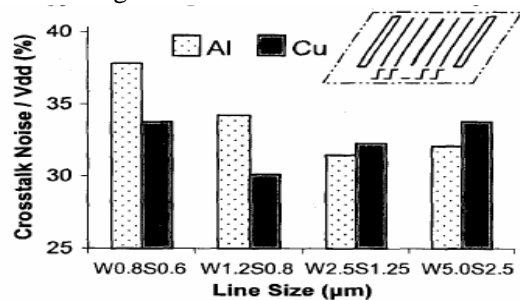


Fig. 4. Crosstalk noise comparison of materials of copper and aluminum

B. Geometric characteristics of shield line and signal lines

The peak noise is analyzed in terms of the coupling length and the shield line width, which are shown in Fig. 5. From this figure, the crosstalk noise for shielded interconnect increases as signal length increases and decreases with the shield width increases.

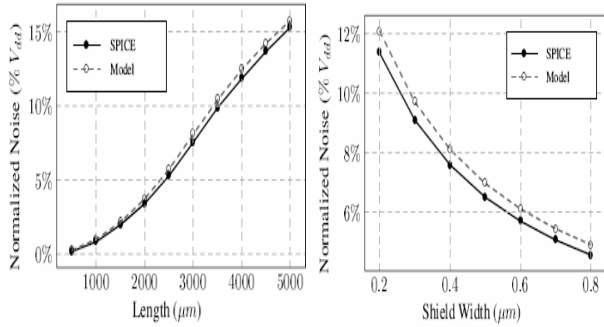


Fig. 5. Crosstalk noise characteristics in term of length of signal line and width of shield line

C. Separation between the signal line and shield line

As the spacing strategy shows, crosstalk noise decreases with the increased separation between two signal lines. Therefore, increasing separation between the shield line and signal line has the same effect.

D. Number of Ground Connections

A shield line is not an ideal ground [6] because the parasitic resistance of the lines exists, which result in the coupling noise in the victim lines. As shown in Fig. 6, the greater the number of ground/power line connections, the smaller the coupling noise on the victim line.

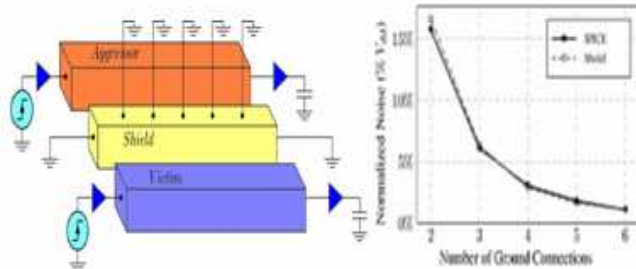


Fig. 6. Crosstalk noise characteristics in term of number of ground/power line connections

E. Shielding Density

Fig. 7 shows the impact of shielding density on signal noise. For inductance-dominant line (W2.5S0.6), it exhibits a more linear function of noise in terms of the number of signal lines between shields than a RC-dominant signal line (W0.8S0.6). Therefore, the optimal shielding number of inductive lines is usually larger than that of resistive lines [2].

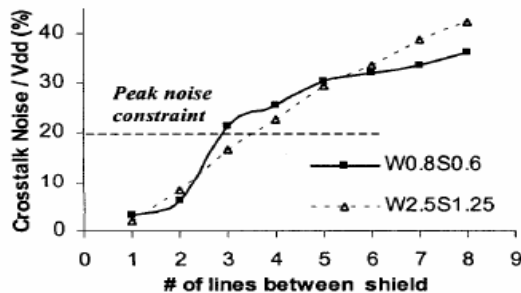


Fig. 7. Impacts of shielding density on signal crosstalk noise

V. SHIELD INSERTION ALGORITHMS

In section 4, the simplified RLC interconnect model is used to analyze the coupling noise in terms of many factors. In practice, however, the circumstances is more complicated because there are hundreds of thousands of signal line which are sensitive to each other and every signal line has its own coupling characteristics. Also, a noise bound to guarantee the no logic malfunction occurs in the worst case should be available for the designer when routing the signal lines. Therefore, we need a shield insertion algorithm to automatically insert the shield lines when necessary. In ideal case, the algorithm minimizes the routing area under the given noise specifications.

Based on the objective above, a simultaneous shielding insertion and net ordering (SINO) problem [7] is formulated to satisfy the given noise bound. The formula-based Keff model, a figure of merit of inductive coupling, is employed to solve specific SINO problems.

First of all, some definitions are introduced in the practical interconnect cases. We define that two nets are *sensitive* to each other if a switching signal on S1 result in the malfunction of S2. The *sensitivity rate of Si* is defined as the ratio of the number of aggressors for Si to the total number of nets.

In addition, there are two important assumptions for developing the algorithm. Inductive coupling exists between any two wires where capacitive coupling only exists between adjacent wires [8]. Based on these assumptions, we can reorder all nets and insert shield to guarantee no sensitive wires are available and we only need to consider the inductive coupling issues in the algorithm.

In order efficiently model inductive coupling effect between two arbitrary wires in the circuit, the inductive coupling coefficient is introduced as a figure of merit which is defined as $K_{ij} = \frac{m_{ij}}{\sqrt{l_i l_j}}$ and calculated as

$$K_{ij} = \frac{f(i) + g(j)}{2}$$

in the practice, where $f(i)$ and $g(j)$ are the linear interpolation function shown in Fig. 8.

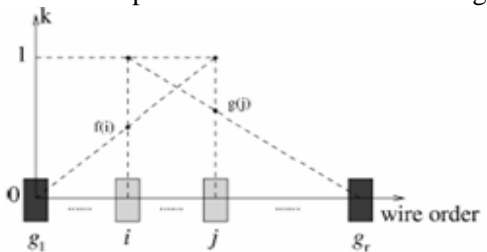


Fig. 8. Illustration of Keff coefficient computation

With the K_{ij} , we can compute the total inductive coupling for S_i as $K_i = \sum_{j \neq i} K_{ij}$ for two sensitive wires, which is very useful parameter in the algorithm.

Based on the Keff model, the SINO noise bound (SINO/NB) problem [7] is formulated as follows: for a given placement P , find a placement P' with the minimum area by simultaneous shield insertion and net re-ordering to make sure and S_i in P' is capacitive noise free and its inductance coupling K_i satisfies $K_i \leq K'_i$, where K'_i is a measure of inductive noise that can be tolerated in S_i to maintain the correct operations.

The shield insertion algorithm (SI) is developed to solve the SINO/NB problem, which is shown in Fig. 9. The basic idea of this algorithm is the following: Run through from the beginning to the end in the give placement P . If two adjacent sensitive nets are found, insert a shield between them. In addition, at each location, we calculate the maximum value of K_i . If K_i is greater than K_{th} , then insert another shield and create a new block.

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SI Algorithm: Given a placement P
for each s-wire  $s_i$  in P at location a:
    if  $s_j$  at location  $P(a - 1)$  is sensitive to  $s_i$ 
        Insert_Shield(a)
     $BC = \text{Compute\_Block\_Coupling}(s_i)$ 
    if ( $BC > K_{th}$ )
        Insert_Shield(a)
     $P(a + 1) = s_i$ 
endfor

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Fig. 9. Shield insertion algorithm to solve the SINO/NB problem

For SI algorithm, we can improve it by firstly running the existing net ordering algorithm to re-order nets to guarantee no sensitive nets are adjacent to each other before running the SI algorithm. This algorithm, called NO+SI, can avoid inserting unnecessary shield and the number of shields can be reduced.

Based on SI algorithm, more sophisticated algorithms such as SINO/SA algorithms, SINO/SPR algorithms and SINO/UPG [9] is developed to get a smaller routing area under the given noise bound. Comparing with these algorithms, the more advanced the algorithm, the less the number of shield is needed. Accordingly, the peak and average noise in the advanced algorithm is greater than that of simpler algorithm. Therefore, the algorithm design is a trade off between the routing area and computing complexity.

VI. CONCLUSION AND DISCUSSION

In this survey paper, shielding methodologies under the signal integrity and routing area consideration is presented for the previous researches and the algorithms to minimize the routing area under the given noise bound is introduced.

For the future researches of shielding methodologies, efforts would be made for the development of two aspects. One is that we need to develop more accurate yet not very complicated RLC interconnect model to analyze and create new shielding strategies (e.g. active shielding [10]) for specific use such as the routing and shielding of clock line and critical signal lines. The other is that advanced shield insertion algorithms based on more accurate interconnect model needed to be developed to estimate the effectiveness of shield insertion and the number of shields needed in the design and further to implement the automation of shield insertion when routing the critical signal lines in the VLSI design industry.

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