Noise-Centric Physical Design Methodologies for VLSI Based Nanoscale Systems

Abstract: Continuous progress in the design and manufacturing of integrated circuits has enabled the integration of more than several billion transistors on the same die with device dimensions in the nanoscale regime. This high integration capability has triggered the era of heterogeneous architectures such as system-on-chip (SoC) and system-in-package (SiP), where diverse circuits are integrated within the same platform. As a result of these improvements, several new design constraints have emerged such as on-chip noise (signal and power integrity), robustness, reliability, and manufacturability. Classical tradeoffs among area, speed, and power have become significantly more complex with the emergence of these physical design constraints, drastically changing the traditional design process. In this talk, current challenges in the physical design process of integrated systems will be summarized with a primary focus on switching noise. Research results in managing on-chip switching noise and its effects will also be presented. For synchronous digital systems, a primary effect of switching noise is variations in the delay, typically referred to as delay uncertainty. Delay uncertainty may cause a system to fail by producing synchronization faults. A methodology will be proposed to reduce delay uncertainty in synchronous digital systems, thereby producing a more robust circuit. For mixed-signal heterogeneous systems, one of the primary concerns is coupling of switching noise to sensitive analog/RF circuits, degrading system performance. A methodology will be described to efficiently estimate the switching noise that couples to sensitive blocks, enabling the reliable integration of diverse circuits. Finally, future research directions will be discussed in the field of next generation heterogeneous embedded systems, both for consumer electronics, as well as physical computing systems.

Biography: Emre Salman received his B.Sc. degree (2004) in Microelectronics Engineering from Sabancı University, Istanbul, Turkey; M.Sc. degree (2006) in Electrical and Computer Engineering; and his Ph.D. degree (2009) in Electrical Engineering, both from the University of Rochester, New York. Since 2009, he has been a postdoctoral research associate at the University of Rochester. His research focuses on design methodologies for high performance, VLSI based digital and mixed-signal circuits with a primary emphasis on noise-centric physical design. He worked as a research intern at Freescale Semiconductor (2006 and 2007), Synopsys (2005), and as an analog design engineer at STMicroelectronics (2004). Currently, he serves on the technical program committee of the ACM Great Lakes Symposium on VLSI (GLSVLSI).