Overview

- Historically, system performance (measured in MIPS or MFLOPS in microprocessors), associated with circuit speed or processing power has been the dominant concern for VLSI designers.

- Second concern has been the implementation area (silicon costs), which affects fabrication yield and packaging -> higher costs.

- The task has been to explore Area-Time balance.

- Until recently, power was an afterthought, designing for maximum performance with whatever power costs.

- In recent years, remarkable growth and success of portable consumer products, such as lap-tops computers, personal digital assistants, cellular phones, pagers, have forced designers to reconsider the design objectives and to take power seriously.

- Average and peak power - a critical concern.
Overview 2

- average power - battery life, weight and size

- peak power - electrical limits of a design, determines the battery type, power distribution network and signal integrity

- excessive heat dissipation triggers different silicon failures and affects the reliability; every 10°C doubles a component's failure rate

- high-end products: DEC 21164, 300 MHz, 3 cm², 50 W 500 MHz, 10 cm², 315 W
Overview 3

- reduced power means reduced heat - positive impact on the environment

- In ultra-low power applications, overall power is held below 1 mW, pace makers, medical implants, wrist watches
The Power Crisis: Heat Dissipation

\[ P = 0.063 \times \text{Area} \times \text{Clock Frequency} \]
CMOS Power Crisis
Note: Run and Sleep mode (5 MW)

Clocked clocks are turned off. 15-30% savings

Power Management Logic determines activity on per cycle basis

Example: IBM 80 MHz PowerPC RISC (3 W @ 3.3V)

• Only minor architectural changes so far.
  Gated clocks, Power-down of non-operational units...

Better Circuit Techniques

Industries is hard to move (microprocessors, memory...)

Reduce Voltage levels from 5V to 3.3V to 2V

Expensive

Reduce chip capacitance through process scaling

The Industry's Reaction
Example: Intel Pentium II Processor

Pentium-2: 8 Watt (3.3V - 133 MHz)
Pentium-1: 15 Watt (5V - 66MHz)
\[
N = \frac{D^2 x PE}{P_{r}} = 50 x 10^6
\]

\[\text{Feature area): } x 100 \]

\[\text{PE (packing efficiency - # of transistors per minimum} \]

\[D^2 \text{ (die area): } x 170\]

\[F \text{ (feature size): } 1/50\]

From 1958 - 1994:

4 times every three years

Rate of increase: 1.5 times/year

Revised:

Number of transistors per chip doubles every year

Moore's Law

Scaling Perspective
Moore's Law
Feature Size
Packing Efficiency
Integration Density

N = D²P/E
Trends in power dissipation