Threshold control.

Reducing subthreshold currents using either low temperature operation (also improves mobility and reduces resistance) or using Silicon-On-Insulator (SOI) technology.
<table>
<thead>
<tr>
<th>Variant</th>
<th>Strengths</th>
<th>Weaknesses</th>
</tr>
</thead>
<tbody>
<tr>
<td>Partially depleted SOI</td>
<td>1. Channel design bulk-like&lt;br&gt; 2. VT insensitive to BOX interface</td>
<td>1. Very susceptible to floating body effects (but solutions are available)&lt;br&gt; 2. Same scaling constraints as bulk</td>
</tr>
<tr>
<td>Fully depleted SOI</td>
<td>1. Elimination of floating body effects&lt;br&gt; 2. Elimination of punch-through currents&lt;br&gt; 3. Elimination of drain-body tunneling</td>
<td>1. VT sensitive to SOI thickness and back interface&lt;br&gt; 2. Back-channel potential may be influenced by drain voltage&lt;br&gt; 3. Difficulty of contacting thin SOI</td>
</tr>
<tr>
<td>Ground Plane (GP)</td>
<td>1. Same as FD SOI&lt;br&gt; 2. GP shields channel from drain&lt;br&gt; 3. GP permits electrical control of VT&lt;br&gt; 4. GP may be used as second gate</td>
<td>1. VT sensitive to SOI thickness&lt;br&gt; 2. Difficulty of contacting thin SOI&lt;br&gt; 3. Degradation of subthreshold slope by close GP</td>
</tr>
<tr>
<td>Double Gate (DG)</td>
<td>1. Maximum electrostatic control of channel and best scaling potential&lt;br&gt; 2. Best current drive and performance&lt;br&gt; 3. GR logic function within single device</td>
<td>1. Difficult to fabricate&lt;br&gt; 2. Mis-aligned top and bottom gates result in extra capacitance and loss of current drive&lt;br&gt; 3. VT control difficult by conventional means</td>
</tr>
<tr>
<td>Stacked SOI (ST)</td>
<td>1. High functional density&lt;br&gt; 2. Shorter wires therefore higher performance and lower power</td>
<td>1. Fabrication complexity&lt;br&gt; 2. Difficult to cool</td>
</tr>
</tbody>
</table>
Interconnects.

- Often ignored in scaling models.
- Has increasing impact on performance and power.

**Cap:**
\[
C = \varepsilon_{\text{ox}} \frac{WL}{T}
\]

\[
S_c = \frac{S x S_l}{S} = S_l
\]

**Res:**
\[
R = \rho \frac{L}{W} \frac{H}{H}
\]

\[
S_R = \frac{S_l}{S^2}
\]

**RC:**
\[
S_{RC} = \frac{S_l^2}{S^2}
\]

But - different scaling to keep resistance under control.

H = constant

Increases fringing

Increases cross-talk
Delay: \( \tau = \frac{CV_{dd}}{q} \left( \frac{1}{V_{dd}} + \frac{1}{V_{dss}} \right) \), Energy: \( E = CV^2_{dd} \)

<table>
<thead>
<tr>
<th>L to minimize</th>
<th>( V_{dd} )</th>
<th>( T_{ox} )</th>
<th>( W_p/W_a )</th>
<th>( W_{p+W_d} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \tau )</td>
<td>min</td>
<td>max &gt;4( V_{i} )</td>
<td>( C_{max}/2 )</td>
<td>max</td>
</tr>
<tr>
<td>( \tau E )</td>
<td>min</td>
<td>( 2V_{i} )</td>
<td>( C_{max}/4 )</td>
<td>1-3</td>
</tr>
</tbody>
</table>

\( C \): total load capacitance, \( C_{ox} \): all load capacitances attributable to gate oxide, \( C_{d} \): load capacitance attributable to driver devices.

<table>
<thead>
<tr>
<th>Gate Length (( \mu m ))</th>
<th>3</th>
<th>2</th>
<th>1.5</th>
<th>1</th>
<th>0.7</th>
<th>0.5</th>
<th>0.35</th>
<th>0.25</th>
<th>0.18</th>
<th>0.12</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{dd} ) (V)</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>5/3.3</td>
<td>3.3/2.5</td>
<td>2.5/2.0</td>
<td>1.5</td>
<td>1.5</td>
</tr>
<tr>
<td>( V_{T} ) (V)</td>
<td>0.7</td>
<td>0.7</td>
<td>0.7</td>
<td>0.7</td>
<td>0.7</td>
<td>0.7/0.7</td>
<td>0.7/0.6</td>
<td>0.6/0.5</td>
<td>0.4</td>
<td>0.4</td>
</tr>
<tr>
<td>( T_{ox} ) (nm)</td>
<td>70</td>
<td>40</td>
<td>25</td>
<td>25</td>
<td>20</td>
<td>15/10</td>
<td>9/7</td>
<td>6.5/5.5</td>
<td>4.5</td>
<td>4.5</td>
</tr>
<tr>
<td>( I_{dss} ) (mA/( \mu m ))</td>
<td>0.1</td>
<td>0.14</td>
<td>0.23</td>
<td>0.27</td>
<td>0.36</td>
<td>0.56/0.35</td>
<td>0.49/0.40</td>
<td>0.48/0.41</td>
<td>0.38</td>
<td>0.48</td>
</tr>
<tr>
<td>( I_{dss} ) (mA/( \mu m ))</td>
<td>0.06</td>
<td>0.11</td>
<td>0.14</td>
<td>0.19</td>
<td>0.27</td>
<td>0.16</td>
<td>0.24/0.18</td>
<td>0.23/0.19</td>
<td>0.18</td>
<td>0.26</td>
</tr>
<tr>
<td>Inverter Delay (ps)</td>
<td>800</td>
<td>350</td>
<td>250</td>
<td>200</td>
<td>160</td>
<td>90/100</td>
<td>70/65</td>
<td>50/47</td>
<td>40</td>
<td>32</td>
</tr>
</tbody>
</table>
1. Double Pass-Transistor Logic CMOS (DPLCMOS)

2. CMOS Low-Voltage Styles:
   - 2. Dynamic BICMOS (dBICMOS)
   - 3. Bootstrap Full-Swing BICMOS (SBICMOS)
   - 4. Sense-Korrel's Bootstrapped BICMOS (SBICMOS)
   - 5. Modified Full-Swing BICMOS (MFSPBICMOS)
   - 6. Dynamic BICMOS (dBICMOS)

CMOS Logic

A Comparative Study of BICMOS and
A Comparative Study of BiCMOS and CMOS Logic
\{00110101\} = \text{Input A}
\{11001011\} = \text{Input B}

Test Input Stimulus

- 3) 1.2V at 0.1-1PF, 4) 1.5V at 0.1-1PF, 5) 3V at 0.1-1PF

B. Fixed Power Supply Voltage with Variable Output Load
   1) 0.1PF at 0.9-3V
   2) 1PF at 0.9-3V
A. Fixed Output Load with Variable Power Supply Voltage

5 Different Test Conditions

CMOS Logic

A Comparative Study of BiCMOS and
A Comparative Study of BiCMOS and CMOS Logic
Power Efficiency at 1pF

2-input NAND, f=50MHz, Cload=1pF

- BFBiCMOS
- BSBiCMOS
- BBCMOS
- dynBiCMOS
- invbCMOS

Power Supply [V]
A Comparative Study of BiCMOS and CMOS Logic

Power Efficiency at 1pF cont.

2-input NAND, f=50MHz, Cload=1pF

- BFBiCMOS
- SRBBiCMOS
- DPLCMOS
- invb CMOS
- MFSSBiCMOS

Power Supply [V]

Power x Delay [UI]
A Comparative Study of BiCMOS and CMOS Logic

Power Consumption at 1pF

2-input NAND, f=50MHz, Cload=1pF

- BSBCiCMOS
- SRRBCiCMOS
- DPLCMOS
- invb CMOS
- MFSSBiCMOS
- BBiCMOS
- BBCiCMOS

Switching Power [μW]

Power Supply [V]
A Comparative Study of BiCMOS and CMOS Logic

Power Efficiency at 0.1pF

2-input NAND, f=50MHz, Cload=0.1pF

---

Power x Delay [f]

0.5 1 1.5 2 2.5 3 3.5

Power Supply [V]

- BFBiCMOS
- BSBiCMOS
- SRBBiCMOS
- DPLCMOS
- Invb CMOS
- MFSBiCMOS
- BBCMOS
A Comparative Study of BiCMOS and CMOS Logic
Power Consumption at 0.1pF

2-input NAND, f=50MHz, Cload=0.1pF

Switching Power [uW]

Power Supply [V]