Recall that the PC (Program Counter) register holds the address of the current instruction being processed. From a logic-design perspective, it can be thought as 32 rising-clock-edge-triggered D flip-flops. (The output of the PC register changes each cycle on the rising edge of the clock.) The Next-PC logic (the Adder, Multiplexor, and branch/jump target and branch/jump inputs to the MUX) determines the PC of the next instruction to be fetched. If the current instruction is not a branch or jump (indicated by a 0 on the branch/jump input to the MUX), then the next PC is simply the current PC incremented by 4. (Because instructions are words we need to increment the instruction address by 4 to get the next sequential instruction.) Otherwise, the branch/jump target input to the MUX is loaded into the PC register. The reset input sets the PC register to all zeros.

Your job is to code this design in VHDL, demonstrate through detailed simulation that your functionality is correct, and hand in a lab report detailing your design and simulation output. Specifics are as follows:

1. Students should work in groups of no more than three. Reports from groups of more than three will not be accepted.

2. Students may choose to work on every aspect of a given project collectively or divide responsibilities among major pieces (e.g., VHDL design, simulation, and report). Whatever works for you is fine, so long as everyone is contributing.

3. A group grade will be given rather than individual grades. All groups must work independently.

4. Note that the picture above is given only to aid in your understanding of how the design works logically. Do not create three different logic blocks and connect them up as shown. Rather, determine how to write a VHDL program that performs the overall function.
5. You must perform a thorough testing of your design using the VHDL simulation tools. Your simulation test plan and results will be an important part of your grade. Think carefully about what inputs you need to thoroughly test each node (connection) in your design. All nodes should be shown in the simulation output that you turn in.

Deadline:


As with homeworks, a 20% late penalty will be assessed for every day the report is late.

Your lab report should include a complete VHDL source code listing, a description of your simulation test plan, and simulation output and discussion.